



Department of Electrical & Electronics Engineering

Course File

Subject: Power Electronic Subject Code: GR15A3018 Academic Year: 2018-19 Regulation: GR15 Year: III Semester: I



Department of Electrical & Electronics Engineering

Course Title: <u>Power Electronics</u>

Following documents are available in Course File.

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7	Course Handout	J	
8	CO-PO Mapping	J	
9	CO-Cognitive Level Mapping	J	
10	Lecture Notes	J	
11	Tutorial Sheets With Solution	J	
12	Soft Copy of Notes/Ppt/Slides	J	
13	Sessional Question Paper and Scheme of Evaluation	J	
14	Best, Average and Weak Answer Scripts for Each Sessional Exam. (Photocopies)	J	
15	Assignment Questions and Solutions	J	
16	Previous University Question Papers	1	
17	Result Analysis	1	
18	Feedback From Students	J	
19	Course Exit Survey	1	
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21	Remedial Action.		J

Course Instructor / Course Coordinator

Course Instructor / Course Coordinator

Karunakumar Davala

D karunakumar

(Name)

(Signature)



Department of Electrical & Electronics Engineering

Vision of the Institute

To be among the best of the institutions for engineers and technologists with attitudes, skills and knowledge and to become an epicenter of creative solutions.

Mission of the Institute

To achieve and impart quality education with an emphasis on practical skills and social relevance.

Vision of the Department

To impart technical knowledge and skills required to succeed in life, career and help society to achieve self sufficiency.

Mission of the Department

- To become an internationally leading department for higher learning.
- To build upon the culture and values of universal science and contemporary education.
- To be a center of research and education generating knowledge and technologies which lay groundwork in shaping the future in the fields of electrical and electronics engineering.
- To develop partnership with industrial, R&D and government agencies and actively participate in conferences, technical and community activities.



GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

Programme Educational Objectives (B.Tech. – EEE)

This programme is meant to prepare our students to professionally thrive and to lead. During their progression:

Graduates will be able to

- PEO 1: Have a successful technical or professional careers, including supportive and leadership roles on multidisciplinary teams.
- PEO 2: Acquire, use and develop skills as required for effective professional practices.
- PEO 3: Able to attain holistic education that is an essential prerequisite for being a responsible member of society.
- PEO 4: Engage in life-long learning, to remain abreast in their profession and be leaders in our technologically vibrant society.

Programme Outcomes (B.Tech. – EEE)

At the end of the Programme, a graduate will have the ability to

- PO 1: Apply knowledge of mathematics, science, and engineering.
- PO 2: Design and conduct experiments, as well as to analyze and interpret data.
- PO 3: Design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.
- PO 4: Function on multi-disciplinary teams.
- PO 5: Identify, formulates, and solves engineering problems.
- PO 6: Understanding of professional and ethical responsibility.
- PO 7: Communicate effectively.
- PO 8: Broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context.
- PO 9: Recognition of the need for, and an ability to engage in life-long learning.
- PO 10: Knowledge of contemporary issues.
- PO 11: Utilize experimental, statistical and computational methods and tools necessary for engineering practice.
- PO 12: Demonstrate an ability to design electrical and electronic circuits, power electronics, power systems; electrical machines analyze and interpret data and also an ability to design digital and analog systems and programming them.

Programme Educational	Programme Outcomes (POs)											
Objectives (PEOs)	1	2	3	4	5	6	7	8	9	10	11	12
1	Μ	М	-	-	Н	-	-	Η	Н	-	Н	Н
2	-	-	Μ	Μ	Н	Н	Н	-	-	-	-	Н
3	-	-	-	-	Η	Η	Μ	Μ	Μ	М	Н	Н
4	-	-	-	Μ	М	Н	Μ	Н	Н	-	Μ	Н

PEOs & POs Mapping

* H: Strongly Correlating (3); M: Moderately Correlating (2)& L: Weakly Correlating (1)

HOD-EEE



Department of Electrical & Electronics Engineering

GRIET/DAA/1H/G/18-19

05 May 2018

ACADEMIC CALENDAR Academic Year 2018-19

III & IV B.TECH – FIRST SEMESTER

S. No.	EVENT	PERIOD	DURATION
1	1 st Spell of Instructions	02-07-2018 to 01-09-2018	9 Weeks
2	1 st Mid-term Examinations	03-09-2018 to 05-09-2018	3 Days
3	2 nd Spell of Instructions	06-09-2018 to 24-10-2018	7 Weeks
4	2 nd Mid-term Examinations	25-10-2018 to 27-10-2018	3 Days
5	Preparation	29-10-2018 to 06-11-2018	1 Week3 Days
6	End Semester Examinations (Theory/	08-11-2018 to 08-12-2018	4 Weeks 3 Days
	Practicals) Regular/Supplementary		
7	Commencement of Second Semester,	10-12-2018	
	A.Y 2018-19		

III&IV B.TECH – SECOND SEMESTER

S. No.	EVENT	PERIOD	DURATION
1	1 st Spell of Instruction	10-12-2018 to 02-02-2019	8 Weeks
2	1 st Mid-term Examinations	04-02-2019 to 06-02-2019	3 Days
3	2 nd Spell of Instruction	07-02-2019 to 06-04-2019	8 Weeks 3 Days
4	2 nd Mid-term Examinations	08-04-2019to 10-04-2019	3 Days
5	Preparation	11-04-2019 to 17-04-2019	1 Week
6	End Semester Examinations(Theory/	18-04-2019 to 08-05-2019	3 Weeks
	Practicals) Regular		
7	Supplementary and Summer Vacation	09-05-2019 to 22-06-2019	6 Weeks 3 Days
8	Commencement of First Semester,	24-06-2019	
	A.Y 2019-20		

Copy to Director, Principal, Vice Principal, DOA, DOE, Balaji Kumar, DCGC, All HODs

(Dr. K. Anuradha) Dean of Academic Affairs



Department of Electrical & Electronics Engineering

2018-19 I sem Subject allocation sheet									
II YEAR(GR17)	Section-A	Section-B							
Special Functions and Complex Variable	Dr GS	Dr GS							
Electromagnetic Fields	SN	SN							
Network Theory	MS	MS							
DC Machines and Transformers	Dr BPB	Dr BPB							
Computer Organization	PRK	PRK							
DC Machines Lab	MP/DSR	PRK/DSR							
Electrical Networks Lab	YSV/GBR	YSV/GBR							
Electrical Simulation Lab	GSR/PS	GSR/PS							
Environmental Science									
III YEAR (GR15)	Section-A	Section-B							
Power Transmission System	VVRR/MP	VVRR/MP							
Microcontrollers	РК	РК							
Power Electronics	Dr TSK	DKK							
Electrical Measurements& Instrumentation (PE-1)	UVL	UVL							
Solar & Wind Energy Systems (OE-1)	PSVD/Dr JP	PSVD/Dr JP							
Sensors/Measurements& Instrumentation Lab	PSVD/PS	UVL/PS							
Power Electronics Lab	PPK/MRE	SN/MRE							
Microcontrollers Lab	RAK/DKK	PK/DKK							
IV YEAR(GR15)	Section-A	Section-B							
Power Semiconductor Drives	YSV	Dr DGP							
Power System Operation & Control	Dr JSD	Dr JSD							
High Voltage DC Transmission Systems	MRE	Dr SVJK							
Electrical Distribution Systems (PE-3)	VVSM								
High Voltage Engineering (PE- 3)	VUR								

2018-10 I sem Subject allocation sheet



Department		Electronics Enginee
Soft Computing Techniques	DAV	DAK
(OE-3)	RAK	RAK
DSP based Electrical Lab	AVK/DKK	AVK/DKK
Power Systems Simulation Lab	VVSM / GSR	VVSM / GSR
Power Electronic Drives Lab	MP/GBR	MP/GBR
I/I BEE(AICTE)	A/B	C/D/E
BEE	ML	
BEE	KS	
BEE	МК	
BEE	MVK	
BEE	MNSR	
Civil II/I (GR15)	А	В
ET	PPK	РРК
M.Tech (PE)(AICTE)	А	
Electric Drives System	Dr DGP	
Power Electronic Converters	Dr TSK	
Power Quality	AVK	
Electric and Hybrid Vehicles	Dr BPB	
Electrical Drives Laboratory	AVK/GBR	
Power Electronics Lab	SN/MS	
M.Tech (PS)(AICTE)	А	
Power System Analysis	Dr JSD	
Power System Dynamics	Dr SVJK	
Power Quality	AVK	
Electric and Hybrid Vehicles	Dr BPB	
Power System Steady State		
Analysis Lab	VVSM/VVRR	
Power System Dynamics Lab	Dr SVJK/YSV	

Department of Electrical & Electronics Engineering

HoD-EEE



Department of Electrical & Electronics Engineering

GRIET/PRIN/06/G/01/18-19

BTech - EEE - B

Wef
III year - I Semester

BTech - EEE - B III year - I Seme										
DAY/ HOUR	9:00 - 9:50	9:50 - 10:40	10:40 - 11:30	11:30 - 12:00	12:00- 12:45	12:45- 1:30	1:30 - 2:15	2:15 -3:00	Roc	om No
MONDAY	PE	PE	MC		SMI Lab / PE Lab B1/ B2				Theory	4404
TUESDAY	PE	PE	MC		MCLab / SMI Lab B1/ B2				SMI Lab - 4507	
WEDNESDAY	PE	PE	PTS	BREAK	EMI SW		WE	Lab	MC Lab - 4505 PE Lab - 4405	
THURSDAY	PTS	PTS	EMI		SV	VE	M	IC		
FRIDAY	PTS	PTS	EMI		М	IC	SV	VE	Class Incharge:	M Lohita
SATURDAY	PTS	EMI	EMI		PELab / MC Lab B1/ B2					
Subject Code	Su	bject Nai	me	Faculty Code	Faculty name		Almanac			
GR15A3016	Power Transmission System		VVRR/MP	V Vijaya Rama Raju/M Prashanth		1 st Spell of Instructions		02-07-2018 to 01-09- 2018		
GR15A2055	Mic	crocontrol	llers	РК	P Prashanth		1 st Mid-term Examinations		03-09-2018 to 05-09- 2018	
GR15A3018	Powe	er Electro	onics	DKK	D Karuna Kumar			2 nd Spell of Instructions		06-09-2018 to 24-10- 2018
GR15A3017		al Measur nstrumen		UVL	U Vijaya Lakshmi			2 nd Mid-term Examinations		25-10-2018 to 27-10- 2018
GR15A3152	Solar & Wind Energy Systems			PSVD/Dr JP	P Sri Vidya Devi/Dr J Praveen		/i/Dr J	r J Preparation		29-10-2018 to 06-11- 2018
GR15A3019	Sensors/Measurements and Instrumentation Lab		UVL/PS	U Vijaya Lakshmi/ P Sirisha		nmi/ P	mi/ P End Semes Examination		08-11-2018	
GR15A3020	Power Electronics Lab			SN/MRE	Syed Sarfaraz Nawaz/ M Rekha			(Theory/ Practicals) Regular / Supplementary		to 08-12- 2018
GR15A2059	Micro	ocontrolle	rs Lab	PK/DKK	P Prashanth Kumar/ D Karuna Kumar			Comm Second	10-12-2018	
HOD					Со	-ordinat	or			DAA



Department of Electrical & Electronics Engineering

	Work Load / D Karuna Kumar										
	9.00 PM	10.00 PM	11. 00 PM	12. 00 PM	1. 00 PM	2. 00 PM	3. 00 PM	4. 00 PM			
MON	Pow	er Elect	ronic								
TUE	Pow	er Elect	ronic								
WED	Pow	er Elect	ronic								
THU											
FRI											
SAT											



Department of Electrical & Electronics Engineering Syllabus Subject— Power Electronics Course Code: GR15A3018

B.Tech III Year I Sem

L:3T:1 P:0 C:4

UNIT-I

Power Semiconductor Devices: Thyristors Silicon Controlled Rectifiers (SCR's) BJTPower MOSFET and Power IGBT and their characteristics and other thyristors Basic theory of operation of SCR Static characteristics Turn on and Turn off methods-Dynamic characteristics of SCR Turn on and Turn off times-Salient points.

Two transistor analogy of SCR R,RC,UJT firing circuits Series and parallel connections of SCR's Snubber circuit details Specifications and Ratings of SCR's, BJT, IGBT - Numerical problems Line Commutation and Forced Commutation circuits.

UNIT-II

Single Phase Half Wave Controlled Converters: Phase control technique, Single phase Line commutated converters, Mid point and Bridge connections– Half wave controlled converters with Resistive, RL load and RLE load Derivation of average load voltage and current Active and Reactive power inputs to the converters without and with Freewheeling Diode Numerical problems

Single Phase Fully Controlled Converters: Fully controlledconverters, Midpoint and Bridge connections with Resistive, RL loads and RLE load Derivation of average load voltage and current Line commutated inverters, semi-converters, active and Reactive power inputs to the converters, Effect of source inductance Expressions of load voltage and current, Dualconverters Numerical problems.

UNIT-III

Three phase converters: Three pulse and six pulse converters Mid-Point and bridge connections average load voltage with R, RL load voltage and current with R and RL load and Semi converter Effect of Source inductance Waveforms Numerical Problems.

Inverters: Inverters Single phase inverter Basic series inverter, parallel Capacitor inverter, bridge inverter Waveforms, Voltage control techniques for inverters- Pulse width modulation techniques Numerical problems. Basics of Resonant Inverters.



Department of Electrical & Electronics Engineering

UNIT-IV

AC Voltage Controllers &Cyclo Converters: AC voltage controllers Single phase two SCR's in antiparallel with R and RL loads, modes of operation of TriacTriac with R and RL loads Derivation of RMS load voltage, current and power factor- waveforms, Numerical problems, Cyclo converters Single phase mid pointcyclo converters with Resistive and inductive load (Principle of operation only) Bridge configuration of single phase cyclo converter(Principle of operation only)Waveforms.

UNIT-V

Choppers: Time ratio control and Current limit control strategies Step down choppers-Derivation of load voltage and currents with R, RL and RLE loads-Step up Chopper load voltage expression. Morgan's chopper Jones chopper Oscillation choppers (Principle of operation only) waveforms AC Chopper Problems.

Text Books

1. P.S.Bhimbra, "Power Electronics", Khanna publications.

2. M.D.Singh&K.B.Kanchandhani, Power Electronics, Tata McGrawHillPublishing company, 1998.

Reference Books

1. VedamSubramanyam, Power Electronicsby New Age International (P) Limited, Publishers

2. P.C.Sen, Power Electronics, Tata McGraw-Hill Publishing.



Department of Electrical & Electronics Engineering

Power Electronics

CO-PO Mapping

Program Outcomes (PO)

- 1. Ability to apply knowledge of mathematics, science, and engineering.
- 2. Ability to design and conduct experiments, as well as to analyze and interpret data.
- 3. Ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.
- 4. Ability to function on multi-disciplinary teams.
- 5. Ability to identify, formulates, and solves engineering problems.
- 6. Understanding of professional and ethical responsibility.
- 7. Ability to communicate effectively.
- 8. Broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context.
- 9. Recognition of the need for, and an ability to engage in life-long learning.
- 10. Knowledge of contemporary issues.
- 11. Ability to utilize experimental, statistical and computational methods and tools necessary for engineering practice.
- 12. Graduates will demonstrate an ability to design electrical and electronic circuits, power electronics, power systems; electrical machines analyze and interpret data and also an ability to design digital and analog systems and programming them.

Course Outcomes of Power Electronics:

- 1. Discuss the basics of power electronic devices.
- 2. Construct the design and control of rectifiers, inverters.
- 3. Discover of power electronic converters in power control applications.
- 4. Compare characteristics of SCR, BJT, MOSFET and IGBT.
- 5. Demonstrate communication methods.
- 6. Experiment the design of AC voltage controller and Cyclo Converter.
- 7. Construct the Chopper circuits.



Department of Electrical & Electronics Engineering CO-PO Mapping

Course	Program Outcomes (PO)											
Outcomes	1	2	3	4	5	6	7	8	9	10	11	12
1	Н	Μ		Μ	Η		Μ		Μ	Μ	Η	
2	Н		Η	Η	Н	Н			Μ		Η	
3	Н	Μ		Μ	Η		Н	Μ		Η		Н
4	Н		Н	Н		Μ	H	Н			Η	
5	Η	Η	Μ	Μ		Η		Μ		Μ	Η	
6	Н	Н	Η	Η		Н	Μ	Η		Μ		Η
7	Н		Η	Н	Η	Н		Η	Μ		Μ	Η

* H: Strongly Correlating (3); M: Moderately Correlating (2); & L: Weakly Correlating (1);

POWER ELECTRONICS

- INTRODUCTION. * Power electronics combine the concepts of power, electronics
- + Power deals with the static and violating power equipme for generiation, triansmission and distribution of electric Power " anoniert beinsteater brie arely themselbert of
- * Electronics deals with the solid state devices and circuits for signal pulcessing to meet the desired control objective * It basically deals with power engineeoring is, generation transmission and distribution and utilization of electrical eneurgy at higher power levels * P.E combines the aspects of electuaries engineering
- where efficiencies is not that important but the principles of control thus play a major viole is controlling power at higher levels and and all addition loss half
- + It is a subject that concerns the applications of electronic puintiples into situations that are mated at pould level rather than signal level.
 - * power electronics is based primarily on the switch. of the power semiconductor devices

"A subject that deals with the apparatus and equipment working on the principle of electronics but vated at paper level matter than signal level.

Some Applications of P.E

1. Acrospace: space shuttle power supplies, satellite power supplies, aincolaft power systems

- 2: Commencial: Adventising, hebting, airconditioning, central oreforigeoration, computer and affice equipment, uninterruptible power supplies, elevators, light dimmeous and flashers 3: Industrial: Airc and industrial furnaces blowers and forms, pumps and compressors, industrial laser, transformer top changeous, violling mills, textile mills, excavators (cenent mills), welding etc.
- excavators) cement mills, welding etc. 4. <u>Residential</u>: Airconditioning, lighting, space heating, refrig-- eviators, electric door openerus, duy evus, fans, personal Computors, vacuum cleaners, elc.
- 5: <u>Tele communication</u>: Botteny changers, power supplies 6: <u>Turansportation</u>: Batteny changers, treation control of electrical vehicles, electric locomotives, streat coros torolley buses, automotive electronics etc.

7. Utility systems: High voltage de transmission(HVDC), excitation systems VAR compensations static circuit breakers, fanss supplementary energy systems (solar, wind). Advantages of Power electronic convertery:-

unit-I (2)

-> Long life el less maintainance due to absence of moving parts.

-> Fast dynamic response of the pre systems as compared to electromechanical converter systems. -> small size and less weight result in less floor space and therefore lower installation cost.

-> mans pocoduction of semiconductor devices has resulted in lower cost of the converter equipment.

Disadvantages:

> they Power electronic converter arcuits have a knowing to generate harmonics in the supply system as well as In the load circuit.

as in the load circuit. > Acto de él ac to ac convertors operate at a low input powerfactor under certain operating conditions > p.e controllers have low overload capacity: > Regeneration of power is difficult in p.e converter systeme:

The advantages possessed by them for outpeightheir disadvantages mentioned above. As a consequence, semiconductor-based conventors are being entreme: extensitively employed in systems where power flow is to be regulat Eased on twom-ond twomoff chairs gate signal requirements idegree of controllability) the Proof semi conductor derices can be chassified as under in Diodes: These are uncontrolled meetifying devices. Their on & after states are controlled by power supply. Thyristors: These bave controlled twom-on by a gatesignal. After thyristors are on they remain blacked-in an-state due to internal inegenerative action & gateloss control these can be tranced off by power circuit.

Controllable subtres: These devices are transdom & transdop by the application of control signals. eg: BJT, MOSFET GTO, SITH, IGBT, SIT & MCT.

Turiac & RCT possess bidirectional connent capebility whereas all other remaining devices (diade, SCRIGTO, BJT, MOSFET, IGBT, SITH, SIT &MCT) are unidirectional correct devices.

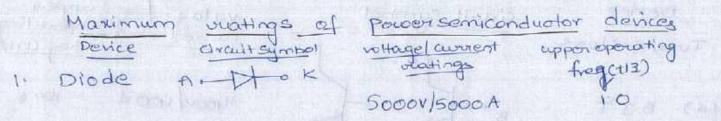
TYPES OF POWER ELECTRONIC CONVERTERS

-> A P.E system consists of one or more p.E converteus -> A P.E converter is made up of some power semiconduction devices controlled by integrated dravits.

-> the P.E (onventors (or circuits) can be classified into

sin types. 1. Diode Rectifier: A diode rectifier circuit Converts ac input Voltage Into a fixed de voltage. The ilp voltage may be single phase or three phase. They are used in electric traction, battery charging, electro plating, power supplies, UPS; voelding etc.

and constant and an endager was first and and the state of



oK

200

25004 500 A 100.0

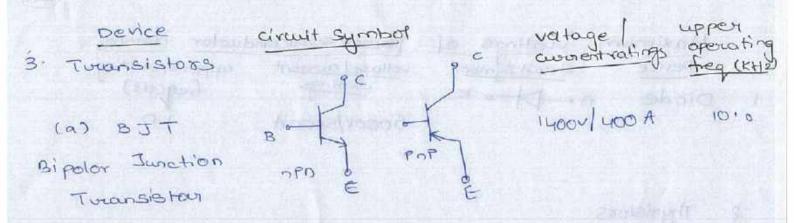
1200V/40A 20.0

1200V/1000A 0.50

0

0

(26)



P

5

PD

S

(b) MOSFET (n-channel)

(D) SIT Go Static Induction transistor

Ċ Gi

(d) IGBT

Insulated make Elpolor translator 1000V/50A 100'0

1200V 300A 100.0

1200 V 500A 50'0

wit-I 3

2: Ac to de converteus (phase - controlled vectifieus): - These convert constant ac voltage to voulable de autput Voltage: these are used in de arrives chemical industries, excitation systems for synchronous machinese

3. De to De conventors (De choppers)

A de chopper converts fixed de input voltage to a controllable de output voltage the chopper ext require forced, or load commutation to twinoff livits -> used in de drives, battory driven vehicles, brolley towers etc.

4. De to ac convertors (inventors)

An inventor converts fixed de Voltage to a varia--ble ac voltage. The olp may be variable voltage or volviable frequency. It requires line, load or forced commutation for twing-eff the tryristors ->use in induction-motor, synchronous motordouves, induction heating, UPS, HVDCT etc.

5. Ac to ac convertous: These convert fixed ac input voltage into variable ac output voltage. These are of two types

as under. (a) <u>Ac voltage controllers (Ac voltage regulators</u>) : converts fixed ac voltage directly to a variable of voltage at

the same frequency. (b) <u>cycloconverters</u>? These circuits converts ilp power at one frequency to output power at a different frequency through one stage convertion. 6. <u>static</u> <u>subtches</u>: The power semiconductor devices can open it as static <u>suitches</u> or contactors: static <u>subtches</u> possess many advantages over mechanical and electromechanical circuit Breakers:

e anapputo to antentra con duppeno

A de chieppen converte l'étent de l'épar volte q le le contrationne de contrat voltage stat chieppen des veguine londeds en toor contrationée le bunnels les puedes als vez bortens contration etheles sector

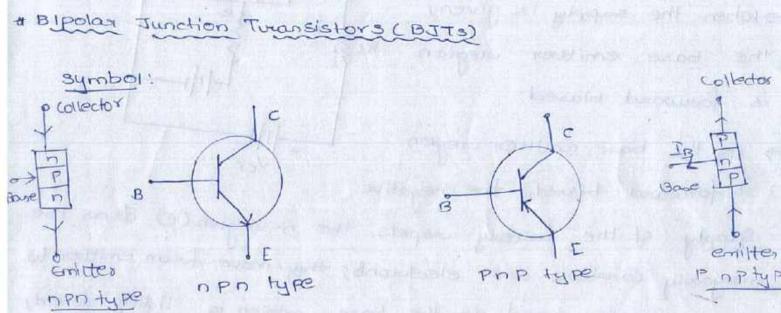
An investor converter and the vertex to vertex to vertex to the sector t

6. At to a convertory i there canned there a time and you with the second part of the sec

Land Ac sothing automore (acting setting setting to a loss a land a setting a setting of setting a land a setting a

the approximation other chically converts in price at a sufficient for any the angle at a different formers the approximation in the price of the convertion in the convertion

POWER SEMILCONDUCTOR DEVICES



> Those layer, two junction npn or pop semiconductor device. > with one puregion sandwiched by two n-regions, npn tra - nsistor is obtained

-> with one two p- regions soundwiched one n- region, Pnp transistor is obtained.

> the term Bipolon denotes that the connect flow in the device is due to the movement of both holes of electrons -> A BIT has three terminals named collectoric), entitlede & Base (B)

-> use of power npn transistors is very wide in very wide in high-voltage and high ament applications. -> BST is amient continuited device. -> PRINCIPLE OF OPERATION:

> NPN -> > when the supply is given, the base emitter sugion is forward blased

> As the base enviter region ______ Vec is forward biased, the negative

Supply of the batteory repets the n-region (E) & as the majority corriers are electrons; they more from emitter to base megion and as the base region is lightly doped, Some of the electrons combine with holes and then remain -ning enter into the collector megion as it is heavily doped and large amount of associat flows in the callector

segion The Base Current IB is given by

The currents IE, IB & Ic are assumed positive when the they enter into the townsistor.

IB

Vbez > Vce,

Vice, Voez

38 stand unlarged

411-100

CHARACTERISTICS Steady state characteristics Input characteristics: The Input characteristics are duraion between the base emilier voltage and base current by keeping

the value of the collector childworldge

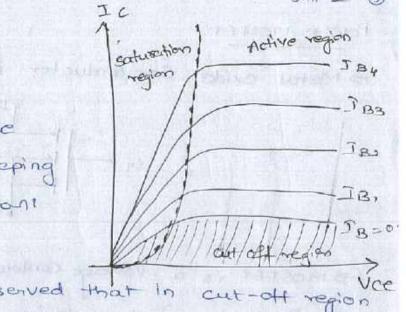
to a constant value.

UNA-I (5)

Output characteristics :

IB4>IB3>IB>>IB1>IB

The output characteristics and drawn between VCE and Ic keeping the base current to a constant value



From the graph, it is observed that in cut-off region the voltage is high and the current is less and in the saturation region , the current is high and the voltag is less:

Switching characteristics In transient condition the forward blased PN'sunction exhibits two parallel copacitances: A depletion layer capacitance and a diffusion copacitance of a reverse blased P-n'suchion has only depletion Capacitance. Under transient conditions, they influence the twing n & two off behaviour of the translates. POWER MOSFET!

definitions to hondulo Semiconductor Field Effecting transistor. > Metal Oxide -> It has three terminals (i) Drain(D) G K (ii) Source(s)

a voltage controlled derice. > MOS FET

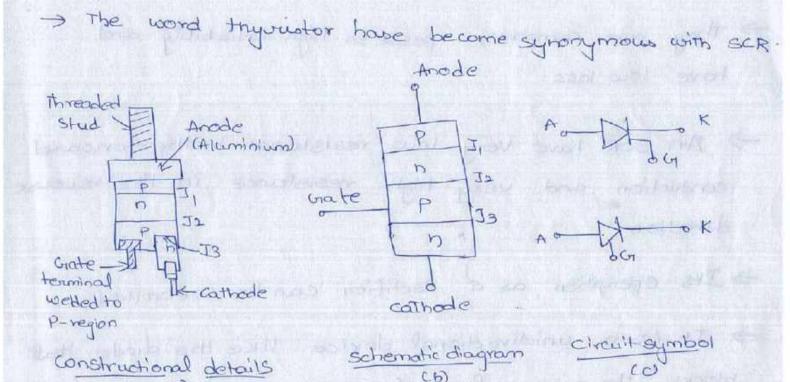
> It is a unipolar device.

-> The Grate circuit impedance in MOSFET is extremely high of the order of 109_2, hence the base current of required in MOSFET is much lesser than the control signal or base current required in BJT. -> The large impedance permits the Moster gate to be driven directly from microelectronic circuits. -> Power MOSFETS are now finding increasing applications in differing and plan series low power high frequency converters > Two types _ > n-channel HOSFET > more commonly used : of higher mobility of electrons. > P-channel MOSFET

THYRISTORS

(0)

> Bell laborraboules were to fabricate a the first silicon - based device called Thy pristor Semiconductor -> An oldestimember thyvis tor of this family, called silicon - controlled most widely Rectifier (SCR), is the used device .



The terminal connected to outer a region is called Cathodelk and that connected to inner pregion is called crote(Gr). > For large current applications, thynistoxs need better cooling, by mounting them on to test sinks.

by mounting them on to test sinks. > SCRS of voltage rating IOKV and an sums current wating of 3000 with corresponding power-handling capacity of 30MW are available.

> They are compact, possess high reliability and have low loss.

> IAM SCR have very low resistance in the forward conduction and very high resistance in the reverse direction:

→ It's a unidivectional device. Like the diode, that blocks the current flow from cathode to anode. → Unlike the diade, a linguistor also blocks the current flow from anode to cathode until it is toggened into conduction by a proper gate signal between gate & cathode

balles at water 1 water of ballantics . I fortunat with a

Puinciple of operation:

- -> The Hyristor operates in three modes
 - (i) Revenue blocking mode
 - (iii) Forward blocking mode
 - (iii) Forward conducting mode

cilReverse blocking mode: -> when carbode is made positive with PJJ = unespects to anode the thyristor is P Chate vievense biased. -> Junctions J1, J3 are oreverse biased. where as J2 is

forward biased. -> The device behaves as if two diodes are connected in Series with revenue voltage applied across them -> A small leakage content of the order of a few mA or ut flows T

unit

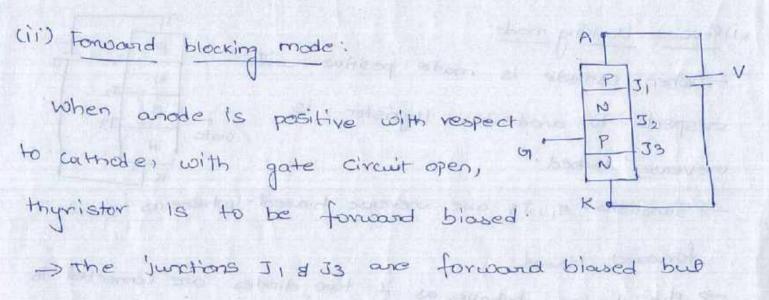
12

-> this is called revenue blocking made, called off-state of the thysistor.

> If the reverse voltage is increased, then at coultical breakdown levels called neverse breakdown voltage VBR, an avalanche occurs at J & J3 & the veverse current increase scapidly.

-> A large current associated with VBR gives vise to note losses in the SCR.

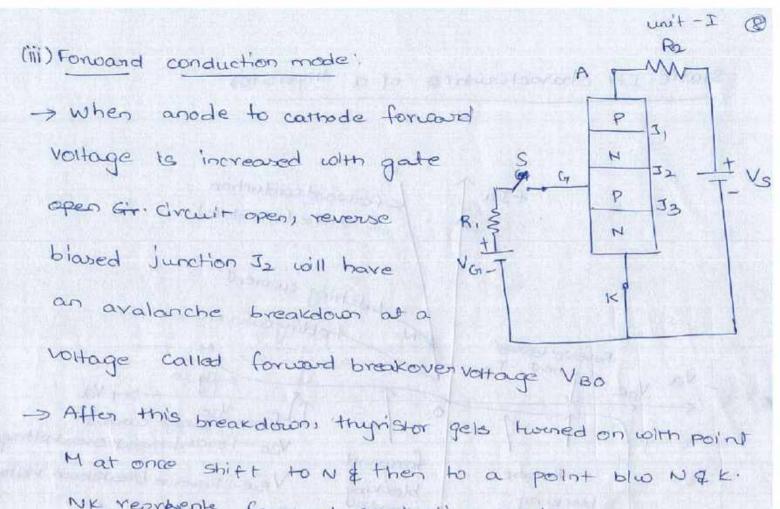
- This may lead to thyristor damage as the junction temperature is may exceed its permissible temperature vulse.
 - > Hence manimum working reverse voltage does not exceed VBR.



Junction J2 is neverse blased.

> In this mode a small lakage current flows called forward leakage current, sore oftens high impedance > : thyristor can be treakted as an open subtch even in the forward blocking mode.

> fit we exceed the voltage beyond the forward break over voltage theo it permanently abroages the device].



NK represents forward conducting mode.

> A Pothysistor can be brought from forwoord blocking made to forward coinduction made by twrning It on by applying (i) a positive gate pulse between gate and cathode

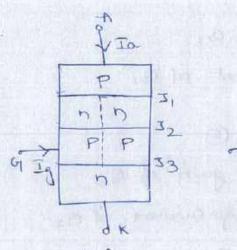
> or (iii) a forcourd break over voltage acutoss anode and cathode.

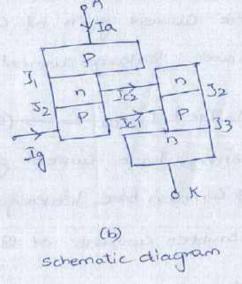
-> when we give the gale current with cathode then the device enters forward conducting mode. (when switch sig closed infi -> In this mode, thyristoris theated as a closed switch.

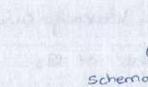
th) Fondand conduction for Static I-V characteristics of a thyristor - Forward corduction +Ia (on-slate) and an ange E mailward current tobling curr end N. Revenue leakage TBO. Ig =0 Va VBR >+ Va TL Forward Leakage curvers 0 note musth E. inochal V30 - Forward break over voltage 2 forward VBR- Reverse breakdown voltag d sta w blocking Ig - gate current Plock 0 -Ja Jack Sol and missinger stori stop by lacq o (i) spot ungo 5 borthod bone accrede apportantes and manua sing sut any au nable and shart pa diffice based a se betond a different is bour side it.

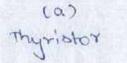
A day Pa

Two transistor model of thyristor.









Two toransistor model

dispi In IBI=Jez

Ig IB2 B2 T

(2)

P 32 102

> The puinciple of thyvistal openation can be explained with the use of its two-townsistor madel (or two transistor

-> The Junctions J1-J2 and J2-J3 can be considered to Constitute prp and npn tocansistors seperately.

-> The Gravit representation of the two transistor model of a thynistor is shown in fig.

-> In off-state of a toronolotor, collector current Ic is crelated to envitter current IE as ist B greadean mi

Jc= «JG+ JCBO

where of is common base current gain

Iceo is the common have leakage awarent of collector-base jurction et a triansistor.

-> from tigic, for os, transistor, IE = anode connert Iq $T_{C} = T_{C_1}$

$$\begin{aligned} F_{C1} = 4F_{C1} + F_{C100} \longrightarrow 0 \\ F_{C1} = 4F_{C1} + F_{C100} \longrightarrow 0 \\ f_{13} \otimes ammon base avoid gain of G, \\ F_{C201} \otimes ammon base avoid gain of G, \\ F_{C201} \otimes ammon base avoid gain of G, \\ F_{C201} \otimes ammon base avoid gain of G, \\ F_{C201} \otimes ammon base avoid gain of G, \\ F_{C201} \otimes ammon base avoid gain of G, \\ F_{C201} \otimes ammon base avoid gain of G, \\ F_{C201} \otimes ammon base avoid gain of G, \\ F_{C201} \otimes ammon base avoid gain of G, \\ F_{C201} \otimes ammon base avoid gain of G, \\ F_{C201} \otimes ammon base avoid for G, \\ F_{C201} \otimes ammon bavoid for G, \\ F_{C201} \otimes ammon base avoid for G, \\ F_{C201} \otimes ammo$$

THYRISTOR TURN-ON METHODS:

> with made positive with respect to cathode, a thyristor can twind on by any one of the following techniques.

Unit-T

(a) Forward voltage toriggeoring

(b) wate turiggering

(d) temperature buiggering

ce) light buiggering.

(a) Forward voltage touggering!

-> When forward voltage 15 applied between anale and cathode with gate chrewit open, Junction J2 is neverse blased.

-> As a viesuit, depletion layer is formed accross Junction J -> The width of the layer decreases with an increase in anode-cathode voltage

>If forward voltage awwas anode-cathode is gradually increased, a stage comes when the depletion layer across J2 Vanishes, J2 is said to have avalanche breakdown and the voltage at which it occurs is called forward Breakove, voltage VBO

> As the junctions J1, J3 are already forward biased, breakdown of J2 allows free movement of capitiens across three i sunctions and as a viesuit, large forward and e-- current flows.

-> The forward current is limited by the load impedance. -> In practice, the triansition forom off-state to on-state Obtained by exceeding VBO is never employed as it may destroy the device.

> VBO is taken as final vortage viating of the device during the design of sce applications

→ After avalanche breakdown, 52 loses its reverse blocking capability: i if anode voltage is reduced below Viso, SCR will continue conduction of the current. → The SCR can now be twened off only by neducing anode current below a certain value called 'holding current'

(b) trate triggering :-

-> This Tuning on of thyristors by gate briggering is Simple, welliable and efficients most usual method. > A positive gate voltage between gate and cathodo is applied.

-> NOITH gat currents a posi changes are injected into the inner Player and voltage at which the forward breakever occurs 18 reduced:

-> The forward voltage at which the device switches to On-state depends upon the magnitude of gate current ->once the scr is conducting a forward current, neverse biased junction II no

longen exists.

-> As such, no gate autorent is orequired for the device to remain in on-state.

lifthe gate content is removed, the conduction of content from anode to calmode remains unaffected.

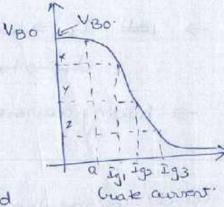
→ If gale current is reduced to zero before the hising anode current attains a value, called the latching current, the thypistor will two-off again.

> The gate pulse width should therefore be judiciously chosen to ensure that anote currient vises above the latching

avosent. -> Latching convent: may be defined as the minimum value of anode avoient which it must attain duoing how -on purocess to maintain conduction when gale signal is remove

> The thysistor can be twined off only if the forward worker fails below a low-level worker called the holding current.

->Holding current' may be defined as the minimum value of anode current below which it must fall for twoming-off the thyristor.



> IL>IH. > Let IL>twoon IH > two off.

> holding current , in industrials applications is almost takenase zero.

- (c) <u>dv</u> toniggeoring.
- -> with forward voltage across the ander and cathode of a thyrites, the two outer junction J1/J3 are forward based J2 is vererse blaced.
- -> J2 has the characteristics of a capacitor due to charges existing across the junction
- -> The space changes cruist in the depletion region resultance
- => Ip forward voltage suddenly applied, a charging current through Junction capacitance (j may two on scr on the
- -> Almost the entire Suddenly applied forward rollage Va appears across Junchion 32

the changing convert ic =
$$\frac{dQ}{dt} = \frac{d}{dt}(G) Va$$

= $C_j \frac{dVa}{dt} + Va \frac{dC_j}{dt}$.

As the junction capacitance is constant, di =0.

inte= cjdVa.

if ante of ruse of forward witage dvalde is high, Ic would be more the period because when more -> This changing amount is play the mole of gate current & turns on the sch even thoughgate signal us zero

-> Note: even if Va is small, it is the mate of change of 1/4 that plays the vole of turing on the device. (d) Temperature tougering:

-> During F.B mode, most of applied voltage appears acoross oreverse junction 32

-> This voltage across, J2, associated with leakage avoient, would vise the tenperature of this junction Dwith Increase in temperature, width of depletion layer decreases. This further leads to more leakage curred 1) athick there. fore, more inclien temperature -> with cumulative process, at some high temperature

(within safe limits), depletion layer of viewerse blowed Junchion variables and the device gets twined on .

12 paras sull 211 - Langa

(e) light triggering ...

→ For light truggered scrs, a necess(orniche) Is made in the Inner P-layer. >It this recers is is is is invadiated, free charge n 33 courriers are generated.

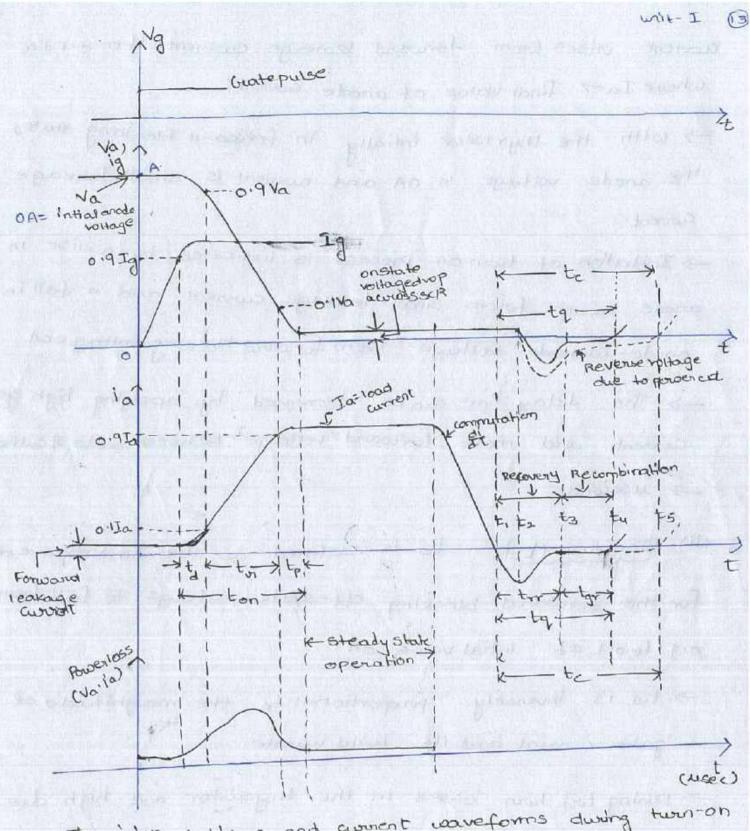
-> If the intensity of this light throws on the receiverceds a certain value, forward biased ser is truned on Wed in HVDCT. (advantage of electrical isolation between power and control circuits)

Twinoff:

-> commutation is defined as the process of twoning-off a trypristog.

Dynamic or switching characteristics of thynistor

-> During turn-on & turn-off publicesses, a thyrustor is subjected to different voltages across it & different converts through it -> The time variations of the nottage across a thyristor of the convert through it during two-on of two-off processes give the dynamic or switching characteristic of a thyristos (a) switching charactuistics during two-on:-Then A transition time forom forward off-state to Sonward on-state called thyristo, turnon time, is defined as the time during which it changes from forward blocking stole to final on-state. -> Tuan-on time can be divided into those intorvals. inderay time to. in the data of and (iii) spread time tp (ii) use time to



Thyoustor voltage and connect vareforms during two-on and two-off processes.

Twinon

is Delaytime ta: ta is defined as the time during which and voltage fails forom one Va to orgva where Va > initial value of anode voltage. (03)

to is defined as the time during which anode

connent vises from forward leakage connent to 0.1 Ia: where Ia-> final value of anode connent.

-> with the thyristor initially in forward blocking states the anode voltage is OA and coverent is small leakage covent.

-> Initiation of twomon process is indicated by a ribe in anode awarent forom small leakage awarent and a fall in anode-cathode voltage from forward blocking voltage of -> The delay time can be decreased by applying high gate Current and more forward voltage between anode exceptioned

-> usecondo.

(ii) Rise time (Ed):- to is defined as the time required for the forward blocking off-state valage to fall from org to oil of initial value off.

-> tor is inversely proportional to the maightfude of gate warmant and its build uprate.

-> During tor, two losses in the thyristor are high due to high Va & Jaigh Ia occuring together in thyristor

(TTP) Spread time (tp) :- tp is the time taken by the anode worked to use from 0.9 to Ia. (or) It is the time for the tonoard blocking voltage to fail from 0.1 to its initial value to on-state drop.

anasonal the need have

wit-I (4)

-> After the spread time, and a connect attains steady state value and the voltage doucp acouss scr is equal to the on-state voltage docop of the order of 1 to 1.5V.

-> Tran on time of an SCR is equal to sum of delay time, visetime and spread time.

-> Total two on time depends upon anode act parameters & the gale signal volveshapes

-> Turn on time can be useduced by using higher values of gate currents.

Scottening characteristics during Turn-off:-

> The dynamic process of the scr from conduction state to forward blocking state is called commutation process or hurs-off process

-> once the thysistor Ison, gate loses control -> scr can be trained off by meducing the anode coment below holding concent:

> The two-off time top of a thypuistor defined as the time between the instant anode courant becomes zero and the instant scr regains forward blocking capability.

-> turn off time is divided into two intowals; vieverly energy time tous and the gate viecovery time tous.

(e.) the toroit the

At instant til ande current becomes zero. > After til anode current builds up in the viewse direction with same dildt slope as before to because of the presence

→ The viewerse viecovery current vernoves excers carriers from J1833 between the instants tielts

-> Revence necovery current flows due to the subserving out of holes forom topp-layer to and electrons from bottom n-layer.

The tay when about 60% of the stored charges are remained forom the outer two layers, carrier density across J, El Js begins to decrease and reverse recovery current also starts decaying

→ It decays fast in beginning but gradual thereater. → The fast decay of recovery current causes a reverse voltage a current the device due to the circuit inductance → This sevence nottage Sunge appears across The thypistor terminals of may therefore damage it. → At to when serverse stecovery avoient fails rearly Bero, Ji 833 recover 8 Sce is able to block the sevence hollage.

witz -05

-> At end of neverse viecovery period (t3-t-), the middle Junction 32 still has heapped block the forward voltage as t3.

-> The changes must decay only by recombination. -> Recombination is possible If a neverse rollage is maintained across SCRI

-> The time for recombination is possible it a se. of changes between to \$ the is called gate recovery time top.

> At try, J2 vecovers of the forward voltage can be reapplied between ande and cathode

>> top (turn-off time) is in range of 3 to loo us.

> ty is influenced by magnitude of forward current, di at the time of commutations and junction temperature dif at the time incoreases with incorease in above 3 factors.

-> If forward current is high before commutation, Imapped changes around Junction 32 are more. -> the fime required for their recombination is more and therefore furn off time is increased.

> The two off-time decreases with an increase in the magnitude of revorse hultage because, it sucks out the courses out of 31 & 33.

> the hum-off time provided to the transistors by the practical circuits is called <u>circuit</u> hum-off time to: -> to is defined as time between the instantanode current becomes zero and the instant neverse voltage due to practical circuit reaches zero.

to > by for reliable two-off. otherwoise the device may two-on at an undesired intant, a process called commutation failure.

-> Thyoustons with slow two-off time (50-100 used) are Called convertor goode sche of too with fast two-off time (3-50 us) are called invertor grade scie.

henogenal with the set to a construction of a with both the the

an pollate the spinor of 210 (and the such) pl

sign of nothernelmouser which not hereinger and altion

and an account on their salastants with the mal dit a

Grate toriggeoring methods

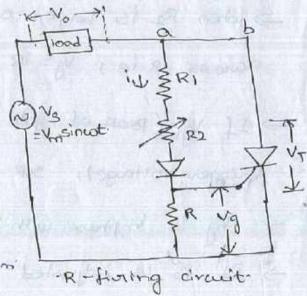
-> Guate triggering is most common method to two-on the sa because this method lends itself accurately for turning on the scr at the desired instant of time.

-> It is an efficient & well able method.

- → By means of gate voltage control, the twining on of the sue can be controlled.
- -> The gate circuit is also called firing or triggering draw (1) Resistance floring circuit:--> It is simple q most economical > Limited mange of fiving angle control (à to 98)) greated dependence on temperature & difference in performance between individual scas are draubbacks which they say

-> R2 is variable mesistance. >If R2 is Beno, gate convert may flow from source, through Was load, RID and gate to cathode.

-> This convent should not exceed maximum permissible gate current Ign



V_mmaximum values

RI can be found forom

Ign Sousierpitage $\frac{V_{m}}{R_{l}} \neq I_{gm} \Rightarrow R_{l} \geq$

the gate convert to a the function of R1 is tollmit safe value as R2 is varied

≥ R should have such a value that maximum valage drop across it does not exceed maximum permissible gate voltage Vgm This can happen only when R2 is zero.

under this condition: $\frac{V_{m}}{R_{1}+R} \cdot R \leq V_{gm}$ $R \leq \frac{V_{gm}R_{1}}{V_{m}-V_{gm}}$

→ As mesistances R, & R2 and lange, gate trigger circuit drows small current

Diode Davous flow of amount during positive half Cycle only. 1e., Ng is half-wave do poulso. The ampli-- tude of this do puse can be controlled by varyings > Potentionneter setting R2 determines the gate voltage amplitude.

Justen R2 is longe, aurent i is small and the rottage across Rie, Vg=iR is also small.

⇒ If Vgp (Reak of gate voltage Vg) is kess than Vgt (gate torigger voltage), sok will not two on. (i.e., Vgp LVgt doesnot transpect with Vs.
⇒ If R2 is adjusted such that Vgp= Vgt, gives x=90° fring angle
⇒ If Vgp>Vgt, as soon as Vg becomes equal to Vgt for first time scr two on a gate loses control and Vg is ineduced to get (almost seve about 1V).
⇒ The fring angle neverbe equal to dever but nearer 1°-4°.

Refining chant .-

> By buying the value of R, fining K-Vot angle can be controlled forom N3 O R2 402 0° to 180°. > T

→ In the negative half cycle, Capacitor C changes through D2 with lower plate positive to the peak supply voltage Vm al which = -9°. Afr

-> After wt=-98, source voltage Vs decoreases forom -Vmat wt=-90° to zero at wt=0°

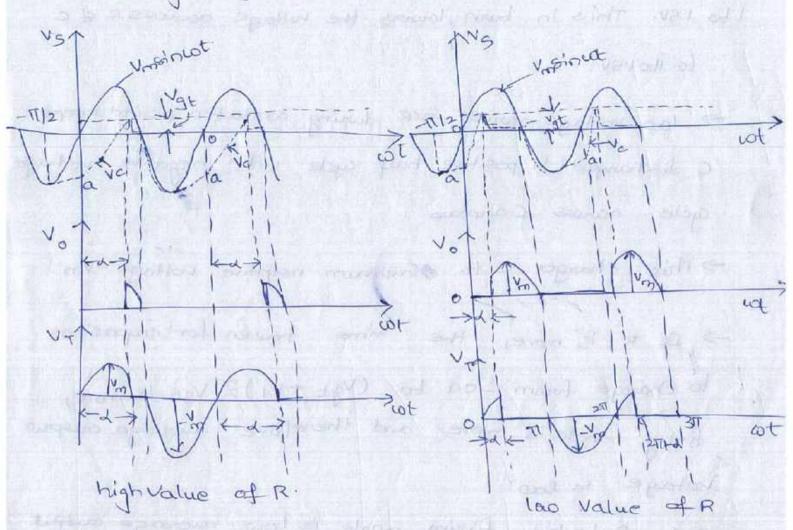
-Vm at cot=-98 to some lower value - on at cot=0°.

> As sex anode voltage parses through Jeve and becomes positive, C begins to charge through R forom the initial voltage - oa at wt=0

-> When capacitor changes to positive voltage equal to gate torigger voltage Vgt, SCR is fired and after this, corpacitor holds to a small positive voltage. -> Diode Q is used to prevent the breakdown of cathode to gate junction through P2 during regarine half cycle.

WIF-I @

> the firing angle can never be zero \$180°.



SOR will brigger when $k = V_{QL} + V_d$ where V_d is the voltage dowop across diode DI''At instant of toriggering) if V_c is assumed constant, the arrient I_{QL} must be supplied by voltage source through R, DI & gate to cathode circuit. max.value of R, $V_s \ge R I_{QL} + V_c$ is given by $V_s \ge R I_{QL} + V_{QL} + V_d$

- when see triggers, Voltage alop across it falls to I to 150. This in two, lowers the holtage across red c to ito 150.

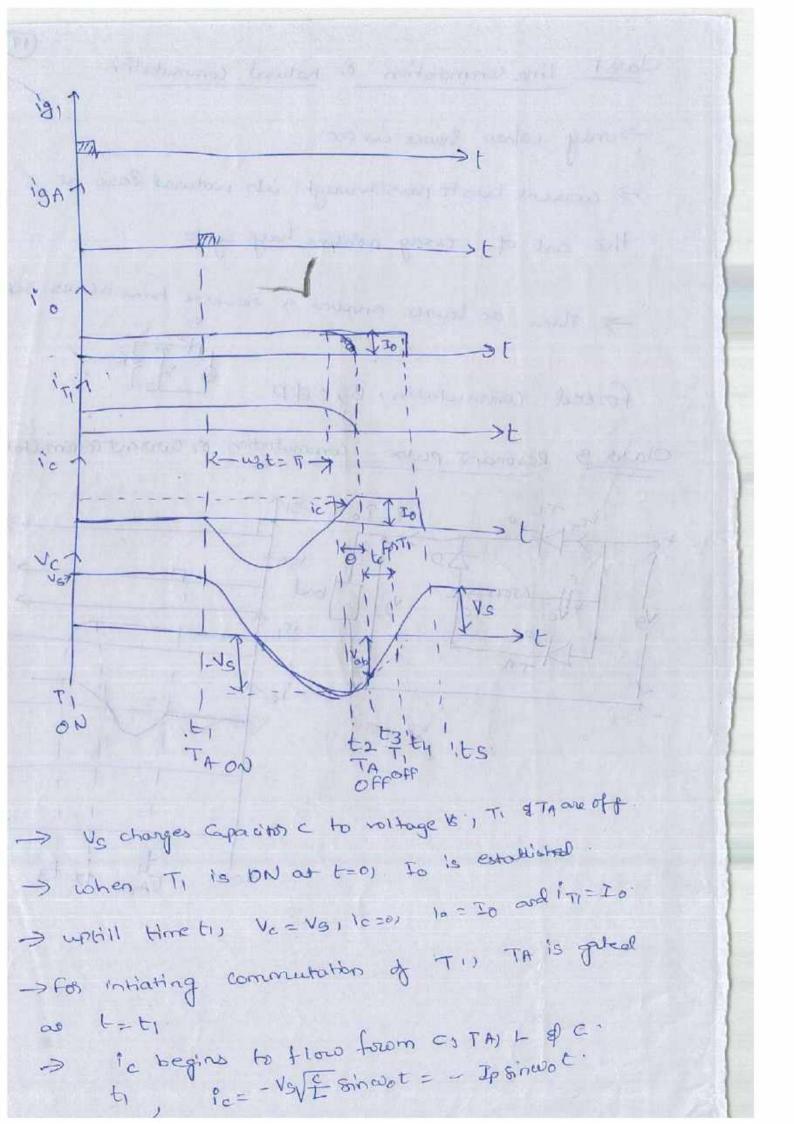
> 1000 voltage across scr during conduction period keeps C discharged in positive half cycle until negative voltage cycle across Campeans

> This changes C to maximum negative voltage - Vm > If R is more, the time taken for capacitor, to change from - on to (Vgt tVd)? Vst is more, firsting angle is more and therefore average output withage is low. > 24 R is less fivring angle is low, average output voltage is more

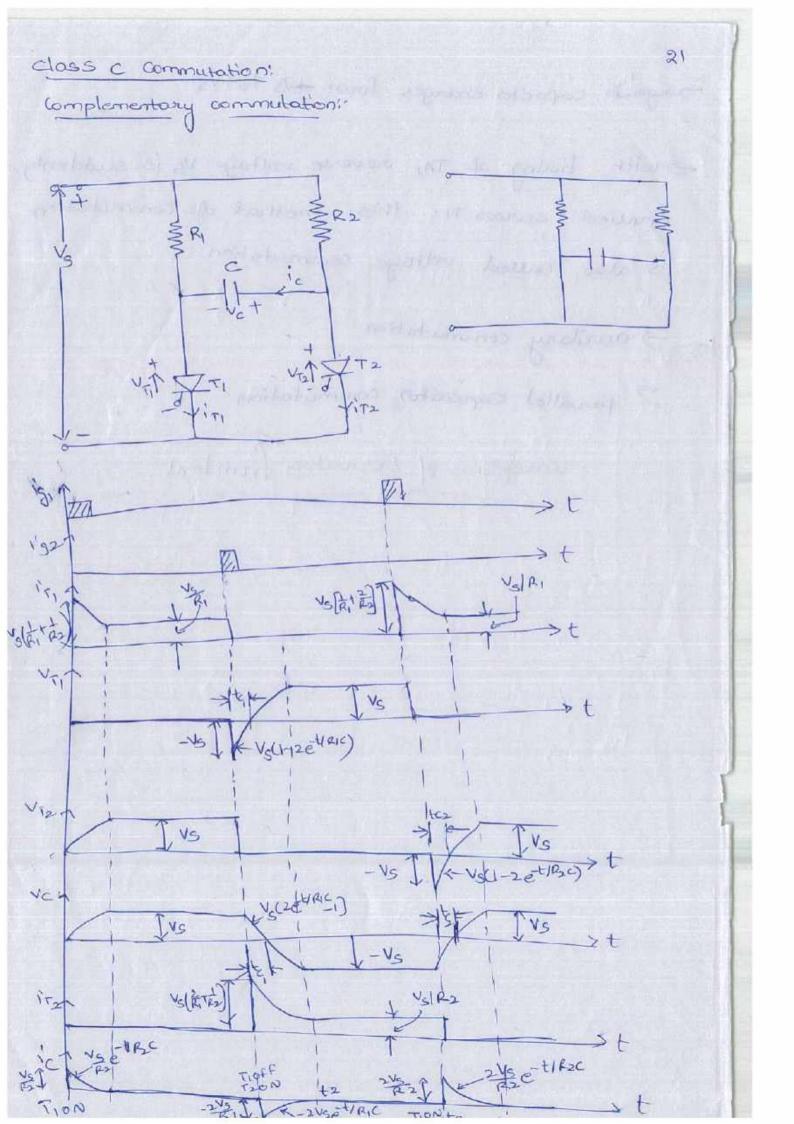
 $e^{V-1}e^{V-2V} \Rightarrow \mathcal{A}$

I'd retrig in 20

19 Clars F Line commitation & natural commitation. ->only when bounce is ac. -> worrent has to parsthrough its natural ferro at the end of every nositive have cycle -> Then ac bource annues a reverse bias actuals scr At it is R forced commutation, B, CEPP Resonant puble commutation of current commutation Class 1917 9-20 ISAroon > bool iti F & guillow at 2 margare TION TAON to to al all the second cover at all such little the



amerate at enjoy at at at



-> again capacitos charges forom +Vs to+Vs

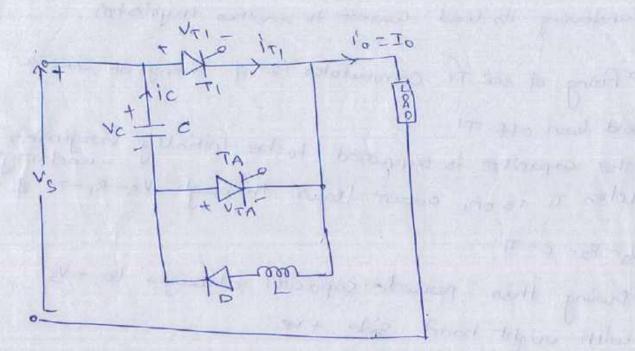
Swith Histing of TA, oreverse voltage Vs is suddenly annued accross TI. this method of commutation is also called voltage commutation.

-> auxiliary commutation

7 parallel capacitor commutation.

courtering of Dormations from dent

class D Commutation: of Impulse Commutation



-> Intially TI & Thrane off -> capacitor is assumed to charged to voltage 's with upper plate the

> where $l_{c=} V_{S} \sqrt{E} Sinvot = 2pointot.$

-> The capacitor discharges from +Vs to Vs. of lower plate becomes +ve > when TA is turned on capacitor voltage Vs applies a revenue voltage accross main thyouiston TI so that VII = - VS & TI is twined OFF.

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> A thyristor carrying load current is commutated by transferring its load current to another trybistos > Fixing of see TI Commutates T2 of fitting of SER T2 would two off TI -> The capacitor is supposed to be initially virginie; unchanged. -> when Ti is on, ament flows through VS-R1-71 & N5- R2- C- Ti. -> During this period capacitor changes to + Vs with night hand side the -> To commutate the main tryvistor, To is twined the copacitor voltage Vc applies on ' -> At this instant, a nevere witage Vs across scr TI and twens it off the manual states in mature I The copacitor discharges through RI-C-T2 the copacitor voltage changes forom Vs to -Vs

I write I - low is The standar

Jerivation part in Pistoinbre tent

2 0 voltage services operation of scr -> when system voltage is more thank using of a single thysiston, scas one connected in series in string -> sees should have their I-V characteristics as close as possible > on account of inherent variations in their characturistics the voltage shared by each see may not be equal La SCRI leakage veristance = V/ 15 high whereas top see , it is low (Valia) 10802 Po a a latornos de Stong Actual voltage avoient moting of the idide stains Storing -[Endividual voltage avvient rating] [number of scession efficiency the string - one scp Derating factor DRF=1-stong efficiency records altres 200 N1+V2 .1 string efficiency = > The two sces can support a max voltage of VitV2 and not the saled blocking rottage 2V1 > A whitem voltage distribution in steady state Can be achieved by connecting a suitable mesistance

acouss each SCR such that each parallel combination has the same resistance.

-> this will require different value of Relistance for each see which is a difficult proposition.

→ A more practical way of obtaining a nearonably withorm voltage distribution during steady state woulding of series- connected scrs is to connect the Same value of shurt nexistance R across each scr. > This shurt resistance R is called the static equalizing circuit.

-> consider 'n' thypistois connected in series -> Let scal has minimum leakage connent Ibmirand each of the remaining (n-i) sees have some leakage correct Ibmir>Ibmi

->scres with lower leakage awrent blocks more Voltage

> As seel has lover leakage aurrent, it will block voltage Vom(say) which is more than that shared by each of the other (n-1) SCRS. Hore Vom is maximum permissible blocking voltage of Seel.

-> scrs do not have identical dynamic characteristics. -> In such a case, series connected scrs will have unequal Voltage distribution during the transient conditions of two-on two-off

> The dynamic characteristics of two sees during two-on are shown where it is assumed that two-on time of sere is more than that of ser]

by std stange total tota

unequal voltage distribution of two services connected to sees during (a) two-on and uptwo-off

> Fig both series one gated, string voltage Vs

is shared as vala by each thyristor. at the some hime, As scel has less two-on time, It gets two-on at instant ti , whereas see 2 is yet aff

 \rightarrow voltage across SCRI drops from V_2 to almost deta \rightarrow At the voltage across off SCR2 will boost from V_2 to Vs.

246

-> Thus voltage shared by two scas are unequal -> After to, voltage & across scar may bound on in case & is greater than its breakover holtage -> scar will get two ed on at time (to table).

>During two-off, scrips assumed to have less two-off time by, than that of scrip inity / 1922 > At instant tz, scrips recovered and is passing through zero voltage whereas scrips is developing

-> At tippiboth sees are developing different verence necevery voltages given by ab for seel & ac for sees. -> so two sees have unequal voltages across them at to -> so two sees have unequal voltages across them at to -> Thus it is seen that sees with different charac--toristics during two-off three suffer from unequal voltage distribution during their two-off process.

of two-oft process

-> A simple sesistor for static voltage equalization cannot maintain equal voltage distribution under transient condition. > During transon of two-oild, the capacitance of neveral biased junctions detormines the nothage distribution across sores in a series connected string.

> As verse blaced jurctions are likely to have different capacitances called self capacitances, the voltage distribution during two-on of two-off periods would be wrequal.

> Voltage equilization under these conditions can be achieved by employing shurt capacitors > This agacitance has the effect of removing the inequalities in thysists' self capacitances.

> In otherwords, dwilling twomon and thom-off periods, the resultant of shurt corpacitance & self Carpacitance of each screwterd to be equal for each of the series connected scres

The choice of Capacitor c is based on the servery chonoctantics of server

-> consider 2 scrs connected in series Tat tc a) flow of R. Rewvent current= DE (D) variation of revenue recovery

(25)0 -> SCRI is assumed to have short revenue recovery time as compared to scr2 -> 00 × 41. St is difference in orderse recovery charges of two SCRSI & 2 -> under this assumption seel recovers first; it there fore goes into blocking state & doesnot allow Parcage of excess change 00 left on sce2. -> This OO, pours through c as shown in fig. > voltage induced by DOS in c, accross scel is <u>Do</u> tohere as no voltage is induced by 008 (= 02-01) in C connected a corross Sch2. \rightarrow : differences in voltages, equal to $0_2 - 0_1 = 0_2$ to which the two shunt Capacitors are changed -> Sari with least recovery time will share highest transient voltage Vbm -> Transient voltage shared by Slow sce2 must be VEM-00 (less than bon shared by fast scri) : Voltage across scr.W= Vbm 11 11 SCR 2, V2- VENT 00 ·· string voltage = Vev, + V2 = Vbm + Vpm _ 20= 2Vbm - 20

=> VS=2Vbr 20 > Vbm=1(VS+20) and V2- Vbm-20 = 1[VS-00] the shing tollage sevenes inpolarity in order to aid the R'R process of series in string > NOW Consider for n-series-connected scles in a string if top scel too characteristics similar to scel & remaining cn-1) sces have characteristics similar to scel & remaining scel would recover first & support voltage Vbm: > The charge (n-1)203 from (n-1) sces would pass through 'c'connected aaross top scel & as result, a voltage > (n-1) 008 could be induced in c

exces is 08.

:. voltage across each one of slow thy ristors is $\left[\lim_{t \to \infty} \frac{-Dq}{c} \right]$ Thus for a connected sers,

voltage across fout top scel, VI = Vbm

(1-1)	31000	thysistow	$= 1.13V_{2}$	
25 65	orta .	policy	= (n-1) [v_m-	1 Acres 1

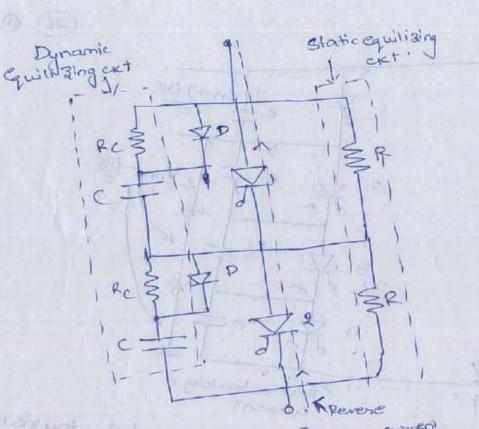
20

is string voltage Ve= V, +(n-DV2 Vbm+(n-D)[Vbm-<u>og</u>] Vbm= th [Ve+(<u>n-D)og</u>] C= (<u>n-D)og</u> Nbm-Vs voltage across Each one of slow scess in terms of

11 11

 V_s is $V_2 = \left[V_{Dm} - \Delta \alpha\right] = \frac{V_s}{n} + \frac{(n-1)\Delta \alpha}{nc} - \frac{\Delta \alpha}{c}$ $V_{2} = V_{3} - \underbrace{08}_{C} + \underbrace{000}_{C} + \underbrace$

(26) 0 6-1)003 5 Perene lookage cument connected thyristow Shing having n-series > During two-off, Vs (source nitage) must rere to aid the neverse recovery current. -> The bransient voltage which each see must be able to withstard is Vom -> The total voltage acting across cet consisting of VS, SCRS h, 3, 2, & topc & pen KUL IS VS+ (n-1) DUS & this must be supported by all scas which is equal to n. Vom. : nVpm = Vst (n-1).00 > Vom= + [Vs+ (1-1).0g] => C= CA-1)20 hVpm-Vs



Reavery aurent Stoken any acel is F.B. state, capacitor connected access it gets change to volhage existing across see that acc. s when this ace is twined on, c discharges heavy awvent twough this ace. For limiting this current spike, a damping mesistor Re is used in series with c. Re also dompsout high frequency additations that may arise due to keyshunt Capacitor d ext inductance.

> combination of RC & C is called dynamic equilising circuit. > RC & C used is to equalise the nothage during dynamic (or transient) conclitions \$ to protect sces against high dyldt

-> when forward voltage appears, diode D by passes Rc during changing time of Capacitos G, makes copacitos more effective in voltage equalization of for limiting du across see. -> During Capacitor discharge Rc corres into play for limiting current spike of dildt.

T (84) Thyou's to protection. ->Policeliable operation of a thysistor, its specified matings must not exceed: -> In practice, a thuriston may be subjected to overvoltage and over awrents. The below of the post ways which of -> During scR twon-on, di may be very large > There may be false truggeoing of scr by high value of du -> A spurious signal across gate athode teaminals may lead to unwanted two-on. -> scrs are very delicate devices, their protection against

abramal operating conditions is, therefore, exertial.

- neighbourhood of the first the whole area of junction. -)trightrouvernt sporeads across the whole area of junction. ->2p the roote of visce of anode current, i.e., dit is longe as compared to the spread velocity of corriers, local hat sports will be formed near the gate connection on account of high averent density. This localised heating may destroy the thyritty.
 - i. di at the time of two-on must be kept below the specified limiting value.
 - -> di can be maintained below acceptable limit by using a small inductor, called di inductor, inservices with anode circuit.

→ Typical didt limit values at scrs are 20-500 Aluse. (b) dv/dt protection: NO.K.T if mate of ourse of suddenly applied voltage accross thyouston is high, the device may get twened on. dv twomon must be avoided as it leads to false operation of thyouston circuit.

→ dv bit course of vuise of forward anode to cathods noting dvaldt must be kept below specified viated limit. Typical values of dubit are 20-500 v1 usec: > False two-on by, dvldt Can be prevented by using a Snubber circuitin parcolled with the device

Design of Snubber circuit: > A snubber circuit censible of a services combination of mesistance Rs and capacitorie Ce In parallel with thrymistor: -> Capacitor G in parallel with device is sufficient to

prevent unwanted duldt truggering of sor.

-> when switch S is closed, a sudden voltage appears across drawit. Cs behaves like a short drawit, therefore across Cs builds up at a slow onate such that duld t awoss Cs & therefore across scr is less than specified maximum duldt mating of the device. -> Before scr is fired by gate pulse, Cs changes to

fue voltage Vs. when scr is twend on , capacitor

Capacitos discharges through the site of sends a current equal to VSI Consistance of local path formed by Cs and SCR). > As this oresistance 18 quite loco, the tuan-on dildt will tend to be excersive and as a vesult, sce may be destroye > Inorder to limit the magnitude of discharge current a resistance Rs is inserted in series with cs of turnon dildt is weduced:

> Rs, is & load circuit parameters should be such that dolds across a during its charging is less than the Specified duldt rating of the SCR of discharge avoient al the two-on of scr is within seasonable limit -> Normally, RS, Cs & load circuit parameters form an underdamped circuit so that duldt is limited to acceptable values. Shubberch Shubberch Ressing Ressi SCR in series with R. Thysistor protection with equation instants is (a) L&RSISS (b) (c) with (all a car and a view) and in -> when s is closed, G behaves like a short cut and ecr In the forward blocking state offers a high revision ce The forward block of the fig (c): ther eq ext is shown in fig (c): for ext (C), $V_{S} = (R_{S} + R_{L})i + L\frac{di}{dt}$ $\rightarrow i = I(I - e^{-t/T}), I - \frac{V_{S}}{R_{S} + R_{L}} \neq T = \frac{L}{R_{S} + R_{L}}$ $\frac{di}{dt} = \frac{d}{dt} (I(I - e^{t/T})) = I \cdot e^{t/T} \cdot \frac{L}{T} = \frac{V_{S}}{R_{S} + R_{L}} \cdot \frac{R_{S} + R_{L}}{L - e^{t/T}}$ = Vs -t/ 2

Value of dildt is maximum when t=0.

$$\begin{pmatrix} \frac{di}{dt} \\ \frac{dt}{dt} \\ \frac$$

Voltage across SCR, Va = Rg. 1

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to patter this bolt and

$$\begin{bmatrix} dVa \\ dt \end{bmatrix} max = \frac{R_sV_s}{r_s}$$

Imar

L. MAST ((SAT) L =

reduced So

-> over convent purotection -> over voltage purotection >dildt protection -> dv/dt purotection

-> brate protection sagainst onervoltages & overcurrents which causes faise touggering of see & damages -> Zenone Zener diode is connected acrurs gate crt -> Resistor connected in series with gate extprovides tratection against over aurents.

22

→ noise can meduced by shielded cables -> Resistor & Capacitor are also connected acruss gate to cathode to by pass noise signals. > c must be less than o'luf of must not detrionate wave shape of gate public

Thysuistor psudection circuit components Snubber circuit overcountert protection di inductor C'B FACLE ARS Supply Grate protection Heatink Transto 1 03 2'D A RIACITI FACLF > Fost acting current limiting tw C'B > circuit Breaken, Z.D -> Zenen diode

(5) -> chen connect punchection anitastand spictor ravise THILS picchetten addations about a pietes descentarios à espetitives renicopose noticataing stade. Anone source is converted and grant Realiston connected in sevires with gave and proces production appind over animate noise convisions by shielded coules soon telasmos our ana ratengo te concest shorp's solan avoid of shitting of the four burn a full of white and sol tought a ct allowing productions and shared making the Harver and Annes DEN A the screenst present in a lost whether the start the second of

STATIC IV characteristics of a thyoustos:

> When During Followed bias Jig J3 -> forward based

J2 -> Reverse blased

> Reserve of depletion layer at J2, does not allow any current to frow through the device

-> only leakage current, negligibly small in magnitude, flow through the device due to the don't of the mobile charges this current is insufficient to make The

-> The depletton layer, mostly of immobile changes do not Constitute any-flow of current

> This is forward blocking state or off state of the + -> The width of the depletion layer at the jurction J2 decreases with the increase in anode to cathod Woltage (Since - The width is inversely proportional to voltage)

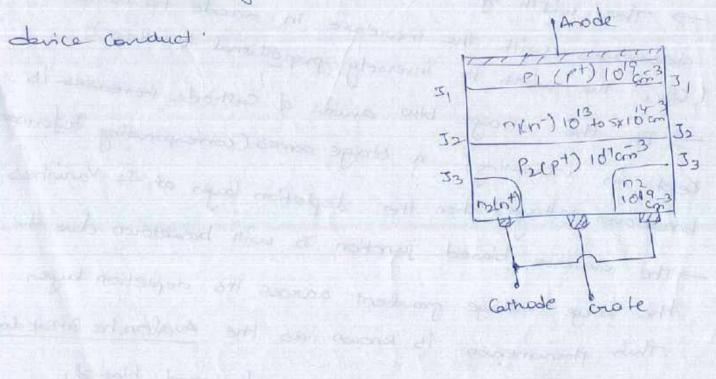
> If the voltage blue and of cathode thereases its tept on increasing, a brage comes (corresponding to forward break over voltage) when the depletion layer at J2 Vanishes -> The onevenue blased junction J2 will breakdown due to

The large voltage gradient aaross its depiction layer This phenomenon is known as the Avalanche Breakdow -> since J1 & J3 are already forward blased, there will be a free Gassier movement across

all the three junctions mesulting in a large amount of council flowing from anode to calhode. > Due to the flow of this forward courset, The device starts conducting El It is then said to re In torressed conducting state or on state.

> when Cathode is made positive corr. to end p byer, J2 becomes Eb, J1 & J3 becomes R'B -> J1 9 32 do not allow any worrent totlaw through ->only a very small amount of leatage current may device. flow because of the doubt of the changes -> The leakage currere is unsufficient to make the

device conduct.

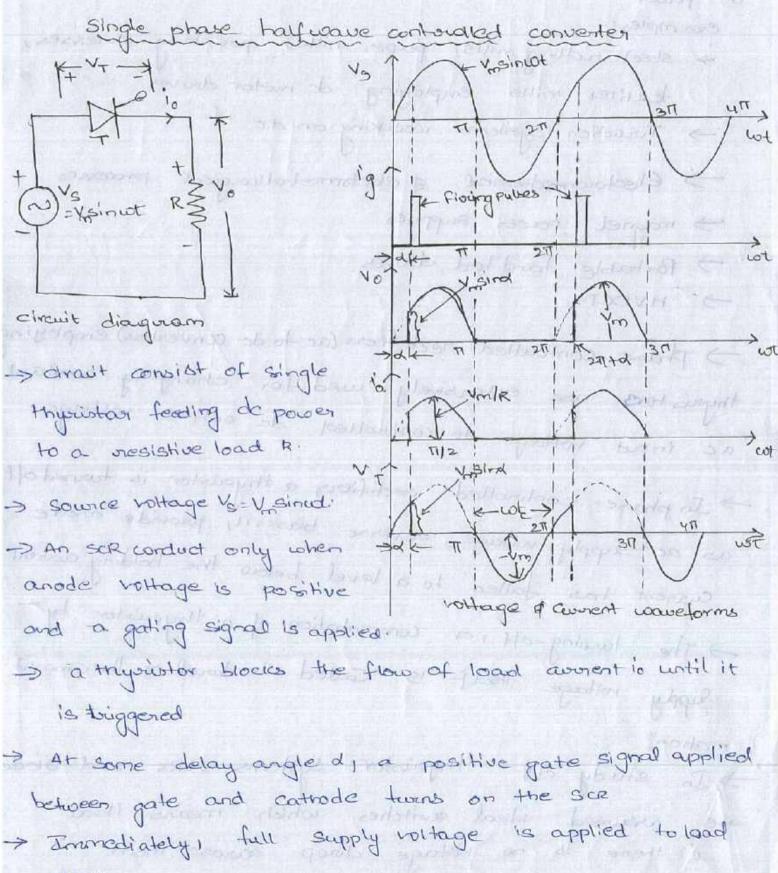




Converters

-> Many industrial applications make use of controllable de power examples !-> steel violling mills, paper mills, pointing presses, textiles mills employing de motor daives -> Turaction systems working on de -> Electoronedienical of electronetraliungical processes > magnet parsen supplies > Portable hand tool doubles > HVDCT. > phase controlled rectifiers (ac to de conventors) employing thypistors are entensively used for changing constant ac input voltage to controlled de output voltage. → In phase- controlled rectifiers, a thyristor is transdoff as ac supply voltage reverse biascrit, provide anode Cuasient has fallen to a level below the holding assurent -> The twining-off 1 or commutation of a thyoristor by Supply rollage itself is called "natural or the commut. -ation", > In study off thyristor systems sere and Diodes are around ideal switches which means that is there is no nottage doup across them

(ii) no veverse courrent exists under veverse roltage conditions (iii) holding avoient is zevo. Turigger draws are not shown for arcuit, for venience



as vo

> At the Instant of delay angle di vo vises forom zero to Vinsing.

→ For resistive lead, account 10 is in phase with Vo.
→ Ruing angle of a thysuistor is measured forom the instant it would start conducting if it were replaced by a lide
→ A fixing angle may thus be defined as the angle between the instant thysuistor would conduct if it were a diade and the instant it is touggered.

> fluing angle may be defined as the angle measured forom the instant see gets forward biased to the instant it is tuggered

→ once sor is on load awarent flower, until It is two-ned-off by versual of nothage at uot=17, 371 etc. → At these angles of 17, 377, 571 ck. load awarent fails to 300 and soon after the supply nothage one versues biases the sce, the device is therefore two-red off.

-> By Varying the firsting angle a, the phase inelation--ship between the start of the load abovent and the supply bottage can be contributed there the torm phase control is used for such a method of contrading the load abovents:

-> A strale phase half-wave circuit is one which produce

only one pube of load awarent during one giple of source voltage

- > Thyoustor conducts from col= & to &Ti, (271+2) to 371, (guta) to si and so on the lange parts
- > over the firing angle delay of, load voltage Vo=0 but during conduction angle (11-2), Vo= Vs
- -> As fiving angle is incureased from zero to T) the average load voltage decireases from the largest Value to zero

handlicky and proved adapted probably -> During, when a to TT, (2TIta) to 3T etc, VT=0 (1to 1'SV) > During tot = The (2TITA), 3TI to (UTITA) etc) VT has the waveshape of supply voltage vs.

VS= VotVT

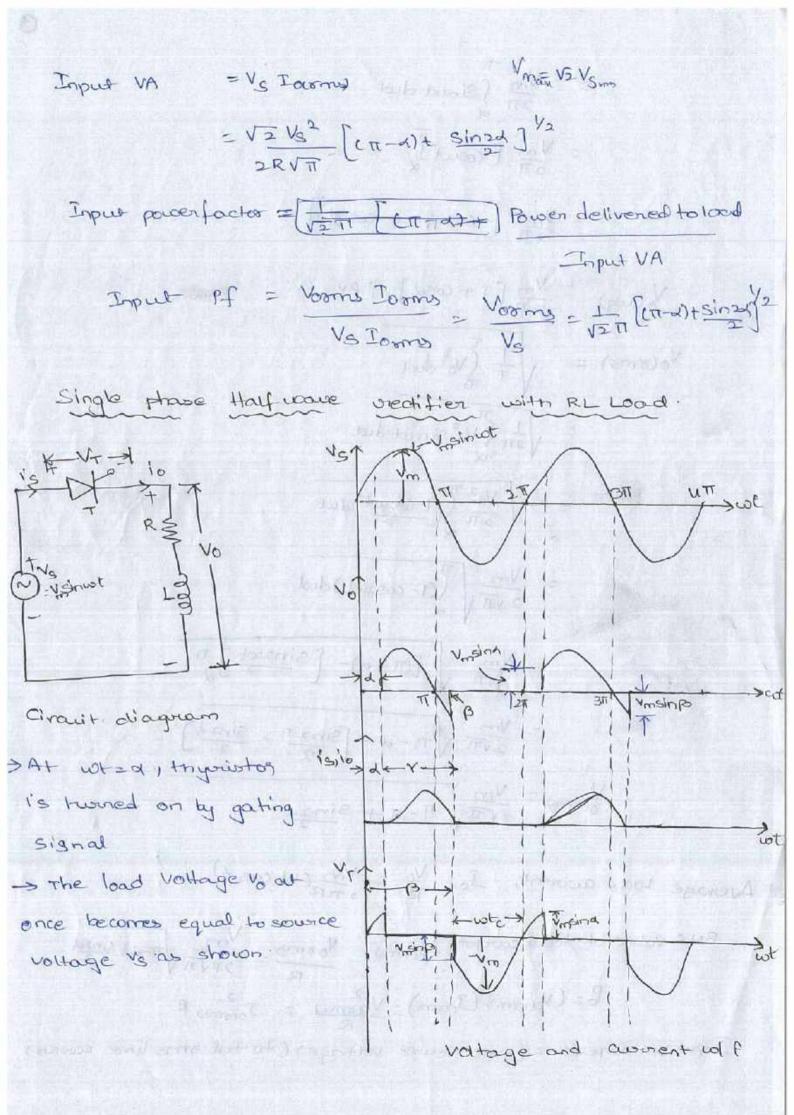
 $V_{s} = V_0 + V_T$ The circult two off time $t_c = \frac{TI}{co} \sec iAs$ see is neverse biased for TI madians

where w= 271f & f is supply friequency in 143. -> The circuit two -off time to must be more than soe two-off time to as specified by manufacturers.

Average voltage Vo

$$V_{0} = \frac{1}{2\pi} \int_{0}^{\pi} V(t) dt = V_{0} = \frac{1}{2\pi} \int_{0}^{\pi} V(t) dt = \frac{1}{2\pi} \int_{0}^{2\pi} V_{0} dt dt dt$$

 $V_{0} = \frac{1}{2\pi} \int_{0}^{\pi} (0) dt + \frac{1}{2\pi} \int_{0}^{\pi} V_{m} sincet d(tot) + \frac{1}{2\pi} \int_{0}^{\pi} V_{0} dt$
 $= 0 + \frac{1}{2\pi} \int_{0}^{\pi} V_{m} sincet dt + 0$



- > But the inductoria L forces the load, or output award is to vive gradually
- > After some time to vieaches maximum value and then begins to dearease:
- → At wt= T, Vo is zero but to is not device because of the load inductance L.
- > After which ser is subjected to menouse anode noting e but it will not be twend off as load current to is not less than its holding accurrent.
 - -> At some angle B>TI, Poincauces to Jerro and sor is turned off as its is alweady ineverse binsed.
- > After wet= B, Vo=0 and 10=0.
- -> At vot= 271+x SCR is toriggered again, vo is applied to bad current develops as before.
- > Angle 'B' is called entinctinction angle and (B-2)=r is called conduction angle.

- and at lot = B, Vr: VmSinB.
 - A B>IT, VI le negative at vot=B.

thus drawit two-offine to = 2II-B sec

Voltage equation for the circuit when T is on, is

The load current is consists of two components, one steady State component is and the other transient component it

Here is is given by

$$P_{S-} \frac{V_{m}}{\sqrt{R^{2}+x^{2}}} \sin(\omega t - \theta)$$

 $\psi = Tar(x)$ $\# x = toL$ $\# is angle by which arms
Generat Is lags Vs'$

Turansient component 1/2 can be obtained from force-force

$$Rit + L \frac{dit}{dt} = 0$$

$$i_t = Ae - (RIL)t$$

$$i_t = Ae - (RIL)t$$

$$\dots \quad i_0 = i_0 + i_t = \frac{V_m}{2} sin(\omega t - 0) + Ae \longrightarrow 0$$

constant A can be obtained from the boundary condition at ust = d.

Thus for eq. (0), $o = \frac{V_m}{2} \sin(\alpha - \phi) + A e^{R \times / LLD}$ $A = -\frac{V_m}{2} \sin(\alpha - \phi) e^{R \times / LLD}$ Substitution of A in eq. (0) gives

It is also seen from the volve form of to that when where B, load current is = a substituting this in eq @ gives $Sin(P-\phi) = Sin(d-\phi)exp\left[-\frac{R}{\omega L}(B-d)\right]$ This townsrendental eqn as be solved to obtain the value of extinction angle B. In case B 15 Known, average load voltage Vo is given by Volang) = $\frac{1}{2\pi} \int V_m sincet dent)$ Humps and A $= \frac{V_{m}}{3\pi} \left[-\cos \omega t \right]_{\alpha}^{B}$ = Vm [-cosp - (-cos]] avenage load voitage V = Vm [cosa - cosp] average bad current To= Vm [cost-cosB]

RMS bad volhage
$$V_{0(sms)} = \left[\frac{1}{2\pi}\int_{x}^{B}V_{m}sinustdtuot\right]^{1/2}$$

= $V_{m}\left[\int_{x}^{B}\left(1-\cos 2\omega t\right)\right]^{1/2}$
= $V_{m}\left[\int_{x}^{B}\left(1-\cos 2\omega t\right)\right]^{1/2}$
= $V_{m}\left[\int_{x}^{B}\left(1-\cos 2\omega t\right)\right]^{1/2}$

1 Inn (and

Rms load current can be found forom eq 3

Single phase Halfwave circuit with RL Load and Free wheeling Piode Vst Vasimul S PT VSO FDA Lagt FTT 271 circuit Diagram A finee wheeling los fly -voheeling) dide is also ifd called by-pass or HT 277 271+2 Commutating diade. > At where, source voltage k model > Is becoming positive. 14-mode II-> At some delay angle a, Voltage à current vouve forms Forward biased scr is triggered and source voltage Vs appears across load as Vo -> At wt= T, source voltage No is zero and just after this instant, as is appears accuse load as we tends to reverse, free wheeling diede FD is forward biased through the the the so the Estro conducting sol

> As a viesult, load current to is immediately transferred from s cr to FD as is tinds to vieverse.

- → At the same time, scr is subjected to reverse blace voltage and zero current, it is therefore burned off at lots Ti. → It is assumed that during Forecohecling(Forperiod, load current does not decay to zero until the scr is briggers again at (2 Tity)
- -> Voltage douop across FD is taken as almost serio, the road voltage vois therefore, serio during the Fulpovia -> the Vocinauit two off time is to=IS sec
- -> The source covert is and thyristor covert it have some nowe form.
- → openation of circuit can be explained in two modes Mode I : this boode also called conduction mode, SCR Conducts from aton, 2πt+2 to 3π and so an & FD is reverse biased. Durbtion of this mode is for <u>T-2</u> sec. → Let the load autent at the beginning of mode I be To → VOLtage equation is Nyshriot: RistLdio. dt ⇒ io: Vm sincut-0) + Ae^(R))t At wt-an io: To sie, at t= to, io: To

$$A = \left[I_0 - \frac{V_m sin(d - \phi)}{J_0} e^{Rd/\omega L} \right]$$

$$i_0 = \frac{V_m sin(\omega t - \phi)}{J_0} + \left[I_0 - \frac{V_m sin(d - \phi)}{J_0} e^{Rd/\omega L} \right]$$

for mode I, d & wt & T

mode II: called freewheeling mode, extends from TI to 27/1td, 3TT to 4TT ta and 50 00:

Jo this mode, SCR is viewerse blased from THOZTISTIONT. -> As the load current is assumed continuous, for conducts from THO(2TI + x), 3T + to (UTT + d) & so on -> Let the current at the beginning of mode I be Io1 as shown.

As bad accorent is passing through FD, withage equation

for mode IL is

$$c = Rio + Ldio$$

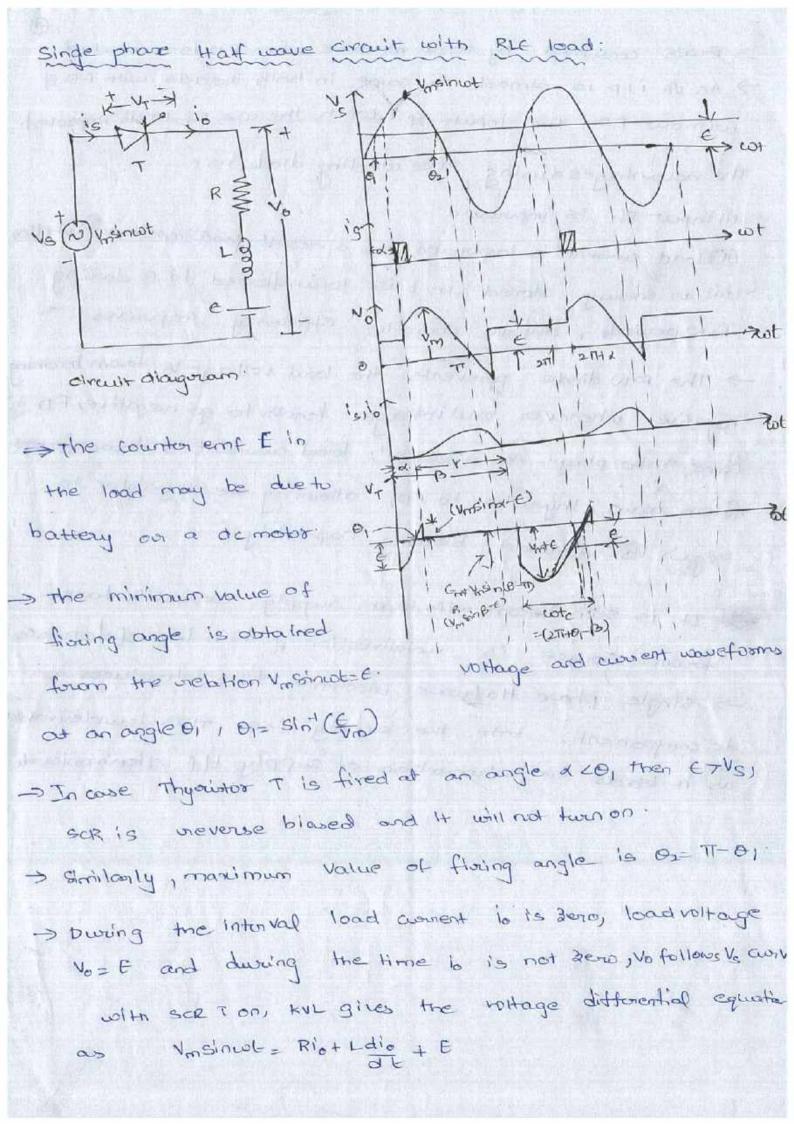
 dt
 dt

For mode II , TI LLOT LLOT + 2)

Avorage load corrent, Io: Vor Vm (1+cosd)

⇒ Load wonert lo is contactbuted by ser forom d to ty (21T+2) to 3T. g '1 '1 '1 '1 by FD forom ato x, TT to (2TT+2) \$\$000 Thus vowe shape of thyristor workt it is identical with wave shape of is for we = d to T, (2TT+2) to 3TT & so on. 111'y, wave shape of FD (worker if j-is identical with with of the

for lot = o to d, TI to (2TIT) and so on:



-> Rover consumed by read is more when FD is connected -> As VA ilp is almost is some in both theorets with FD g without FD, the input pf with the use of FD is improved. The advantages during Force cohecting diade are

dilinput of is imprived. (il) load convert is importance as a mesual load impedance is betto, (iii) as enougy stored in L is tocansferred to R during F. 10 periode, overall converter officiency importones. -> The FIN diode prevents the load voltage 16 forom becoming negative: whenever bad voltage tends to go negative. FD come into play. As a nexult, load convent is townstewed forom main thyristor to FD, allowing the thyristor to oregain its forward blocking capability.

-> It is seen from with that supply about is taken forem source is unialivection of 15 in form of de pueses -> single phase Halfware mechifier thus introduces a de component into the supply line. This isurelesivable as it leads to saturation of supply the ellownomics etc in normal has view at first dissiding adoption in the

The a state prover it with an anteren plackage

agailer track and and how a that deviated and ground a

3 + 3 the state - surplarate - in

The solution of the equation have steady state content component is and the transient content component "t" is is sum of is (steady state content due to ac source rollage acting alone) and is 2 (due to de counter emp E acting alone).

is, due to source voltage Vinsinwel's given by

If only & were present, is = - E

$$1s_2 = -\frac{E}{R}$$

transient current it is given by it-AEEt. Total avoient is is given by is=is_tisztik = Vm sincet-o)- fraely At $\omega = \alpha$, $i_0 = 0$ ie, at $t = \frac{\alpha}{\omega}$, $i_0 = 0 \Rightarrow A = \begin{bmatrix} \epsilon & V_{msinkled} \end{bmatrix} \begin{bmatrix} Rd \\ e^{L\omega} \end{bmatrix}$ $\frac{1}{100} = \frac{V_m}{2} \left[since(-\phi) - sin(d-\phi) exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - exp \left\{ -\frac{e}{\omega L} (\omega t - d) \right\} \right] - \frac{E}{R} \left[1 - \frac{e}{R} \left[1$ eq O is applicable for a guot g. The entirchion angle B depends upon load enf E, fring angle & & load d=ran'(wil) Average voltage accuss inductor is zero. Average load current Io = 1 [S(V_msincot - E)dcuot)] = 1 R [Vm(cosd-cosB) - E(B-d)]= Here conduction angle r= B-d. Putting B= rtding@

$$J_{0} = \int_{\pi R} \left[V_{m} \left\{ cosd - cos(Y+x) \right\} - E \cdot Y \right]$$

$$J_{0} = \int_{\pi R} \left[E_{m} sin \left[d + \frac{v}{2} \right] sin \left[\frac{v}{2} \right] - E \cdot Y \right] \left[cost \cdot cosy = 2sin \frac{1}{2} t sin (x + \frac{v}{2}) \right]$$
Average bad voltage $V_{0} = E + J_{0}R$

$$= E + \frac{1}{2} t \left[E_{m} sin(x + \frac{v}{2}) sin \frac{v}{2} - vC \right]$$

$$\therefore V_{0} = E \left[1 - \frac{v}{2} t \right] + \frac{V_{0}}{\pi} sin(x + \frac{v}{2}) sin \frac{v}{2} - e_{p} \left(\frac{v}{2} \right)$$
Average voltage V_{0} can also be obtained as
$$P = \frac{1}{2} t \left[\int_{-\infty}^{0} V_{m} sin(x + \frac{v}{2}) sin \frac{v}{2} - e_{p} \left(\frac{v}{2} \right) \right]$$
Average voltage V_{0} can also be obtained as
$$P = \frac{1}{2} t \left[\int_{-\infty}^{0} V_{m} sin(x + d \cdot d t) + E(3\pi + d - B) \right]$$
Average voltage V_{0} can also be obtained as
$$P = \frac{1}{2} t \left[V_{m} (sin(cs, d - cos P) + e(2\pi + d - B) \right]$$

$$V_{0} = \frac{1}{2} t \left[\int_{-\infty}^{0} V_{m} sin(ct, d \cdot d t) + E(3\pi + d - B) \right]$$

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$$V_{0} = \frac{1}{2} t \left[\int_{-\infty}^{0} V_{m} (sin(cs, d - cos P) + e(2\pi + d - B) \right]$$

$$V_{0} = \frac{1}{2} t \left[\int_{-\infty}^{0} V_{m} (sin(cs, d - cos P) + e(2\pi + d - B) \right]$$

$$I_{0} = \frac{1}{2} t t \left[\int_{-\infty}^{0} V_{m} (sin(cs, d - cos P) + e(2\pi + d - B) \right]$$

$$I_{0} = \frac{1}{2} t t R \left[V_{m} (sin(cs, d - cos P) + e(2\pi + d - B) \right]$$

$$I_{0} = \frac{1}{2} t t R \left[V_{m} (sin(cs, d - cos P) + e(2\pi + d - B) \right]$$

$$I_{0} = \frac{1}{2} t t R \left[V_{m} (sin(cs, d - cos T - 0) - E(\pi - (B + \pi)) \right]$$

$$R_{m} = \frac{1}{2} t t R \left[V_{m} (sin(cs, d - cos T - 0) - E(\pi - (B + \pi)) \right]$$

$$R_{m} = V_{0} = \frac{1}{2} t t R \left[V_{m} (sin(cs, d - cos T - 0) - E(\pi - (B + \pi)) \right]$$

$$I_{0} = \frac{1}{2} t t R \left[V_{m} (sin(cs, d - cos T - 0) - E(\pi - (B + \pi)) \right]$$

$$R_{m} = \frac{1}{2} t t R \left[V_{m} (sin(cs, d - c$$

$$I_{0x}^{2} = \frac{1}{2\pi R^{2}} \int_{x}^{B} (V_{m}^{2} \sin^{2} \cot t + E^{2} - 2V_{m} E \sin \cot) d(uot)$$

$$I_{0x} = \left[\frac{1}{2\pi R^{2}} \int_{x}^{B} (V_{0}^{2} + e^{2}) (P_{0} - x) - \frac{V_{0}^{2}}{2} (\sin 2P_{0} - 2\sin 2x) - 2V_{m} E(\cos x - \cos P_{0})\right]$$

$$P_{0x} \cos t delivered to load, P = I_{0x}^{2} R + I_{0} t$$

$$Supply P_{0x} \cos t factor = I_{0x}^{2} R + I_{0} t$$

$$At \quad \omega t = 0, V_{5} = 0 \quad \text{and therefore } V_{T} = E \cdot$$

$$At \quad \omega t = 0, V_{5} = E \quad \therefore \quad V_{t} = 0$$

$$At \quad \omega t = 0, V_{5} = E \quad \therefore \quad V_{t} = 0$$

$$At \quad \omega t = \alpha, \quad V_{5} = V_{m} S \ln \alpha \quad \therefore \quad V_{t} = V_{m} S \ln \alpha - \epsilon$$

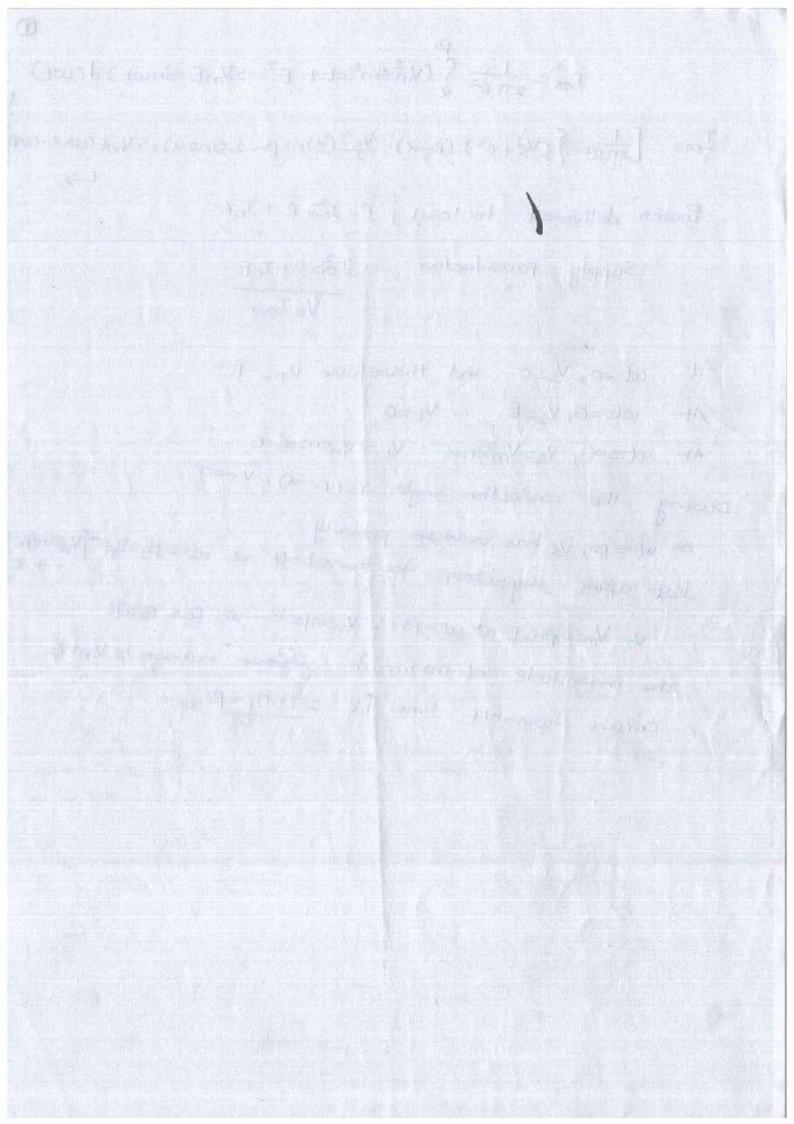
$$During \quad the conduction angle \quad Y_{m} (B - \alpha), \quad V_{T} = 0$$

$$At \quad \omega t = \beta, \quad V_{5} \text{ has oreverse placed } Y_{m} = B, \quad V_{T}^{-} [V_{m} S \ln (B^{-T})]$$

$$U_{T} = V_{m} S \ln p_{0} - E \text{ at } u_{t}^{2} = B_{1} \therefore \quad V_{m} S \ln \beta \text{ is -ve for } B > T$$

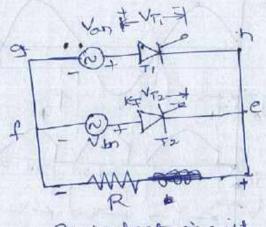
$$The magnitude of maximum oreverse voltage is V_{m} t \in B$$

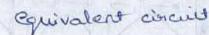
$$The magnitude of the V_{m} = V_{m} S = 2\pi + \theta_{1} - B \sec$$



Single phase Full vouve conventers. ->single phase full wave mid-point Converter Von=-Van second wit TT2 TI+0 211 ptito TT Ti > K-T2 + F-TIcircuit diagram TEtal -> The cit dlagam vt. Javisink ! of a single phase fullwave -Jun, convertor using a centure--tapped Hf is shown VT2 swhen terminal a 1s positive when y "Justor" with mespect ton, terminaln St is positive with nespect to b. -22/00 :. Van= Vnb on Van= -Vbn as n is midpoint of secondary voltage and current woweform winding. -> Thyristor Ti is forward blased during positive half uple degative 11 and thyriston T2 is forward " these are therefore toniggered a coordingly. -> At wt=0, Van is positive, Ti is : forward biased and longened at delay angle &, Ti gets twined on -> At this firing angle &, Supply rollage 2VmSind never biases I, this sce is inturned off

Hene Ti is called incoming thyrists & Tz is outgoing thyrists -> As incoming see Ti is triggened, ac supply voltage applies reverse bias across the outgoing thyrists and transit off.





Van = Vinsinut Vbn = - Vnb = -Vinsinut Nab = Van + Vnb = 24h sinut when whether a transferred sch T2 wis pubjected to a viewerse vortage Vab 24psind auxient is transferred for T2 to T1 of and as a result T3 is twined off · Voltage acousts T2 can also be obtained by applying KVL to the loop efghe of the equivalent circuit at the instant T3

is touggeored. $V_{T2} - V_{bn} + V_{T1} = 0$ $\Rightarrow V_{T2} = V_{T1} = V_{T1} - V_{an} + V_{bn}$ $\Rightarrow V_{T1} = 0$ when T_{1} is conducting $V_{T2} = 0 - V_{m} \sin \alpha$ $\Rightarrow V_{T2} = -2V_{m} \sin \alpha$. NUM At $wt = \pi + \alpha$, T_{2} is touggened, T_{1} is viewerse biased by NOHage magnitude $2V_{m} \sin \alpha$

The londwebs form a to
$$\pi + \alpha$$

At wet = π_1 , π_1 is uneverse biased that by voltage $2V_{12}\sin \alpha$.
At wet = $\pi_1 + \alpha_1$, π_2 is thriggened
At wet = $\pi_1 + \alpha_1$, π_2 is thriggened
At wet = $\alpha + \alpha_1 + \alpha_2$.
For π_2 , $t_2 = \pi_3$ sec
 π_1 , For π_2 , $t_2 = \pi_3$ sec
 π_1 , T_2 , $t_2 = \pi_3$, $T_3 = \pi_3$ sec
 $V_0 \cos \alpha_2$ = $\frac{1}{\pi_3} \int V_{12} \sin \alpha_1 + \cos \alpha_1$
 $= V_{12} (-\cos \pi - \cos \alpha)$
 $:V_{0000} = \frac{1}{\pi_3} \int V_{12} \sin \alpha_1 + \cos \alpha_1$
 $= V_{12} (-\cos \pi - \cos \alpha)$
 $:V_{0000} = \frac{1}{\pi_3} \int V_{12} \sin \alpha_1 + \cos \alpha_1$
 $= V_{12} (-\cos \alpha_1 - \cos \alpha)$
 $T_0 \cos \alpha_1$; $V_{0000} = V_{0000} = V_{1000} (1 + \cos \alpha)$
 $T_0 \cos \alpha_1$; $D = (-\frac{1}{\pi_3} \int V_{12} \sin^2 \alpha_1 + \cos \alpha_1)$
 $= (V_{12} \int (-\cos \alpha_1 + \sin \alpha_2 - \sin \alpha_1) \int V_{12}$
 $= (V_{12} \int (-\cos \alpha_1 + \sin \alpha_2 - \sin \alpha_1) \int V_{12}$
 $= V_{12} \left[(\pi - \alpha) + \sin \alpha_2 - \sin \alpha_1 - \sin \alpha_2 - \sin \alpha_1 - \sin \alpha_2 - \sin \alpha_1 - \sin \alpha_1$

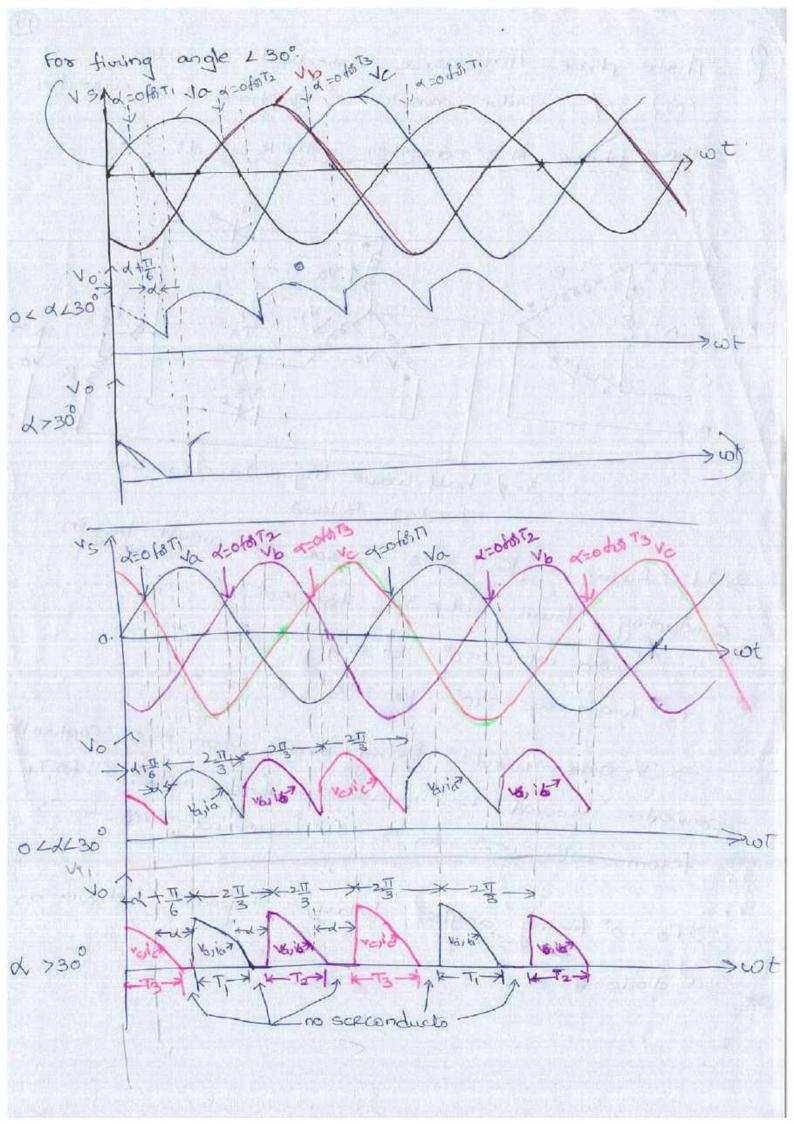
bear of the guard !

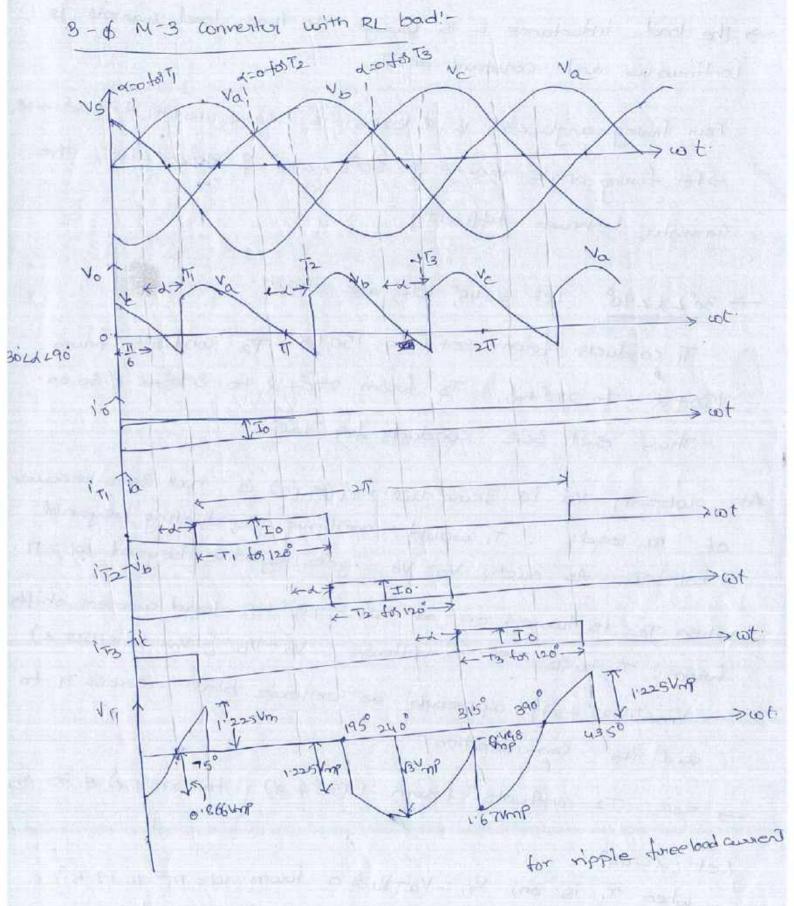
 \rightarrow t_c > t_q.

0

Single phase Midpoint converter with RL load. fall wave Von bo Nan NS E Ubni Vó wit > At wet = 0, Van istve. Ti -> FB & at d, It gets two ned on i6 col & To stevene blases by 2 VmsInd VTI 12Vinsing el twined off. 20t > After w(= x) T1 conducts 24,515 -2Um of to TT+d trom VIE zvosir > A+ wt = TI, Ti viewerse biased Swit but will continue conducting as -> At wt= T+d, T2 is briggered, T, is vie reverbiased rollage T2 is not get gated. magnitude 2Vm stnd, current is transferred from T1 to T2: Ti is : twend off \rightarrow At wt= d, T2 is oft) tc = $\frac{T_1-d}{W}$ \rightarrow At $\omega t = \pi + d = T_1$ is off) $t = 2 \pi - (\pi + d) = \pi - d$ Volang) = ITS Vm sinual duot) = Vm (-loswer) TItal $= \frac{V_m}{T} \left(-\cos(T + d) + \cos d \right)$ Volaug) = 2Vm cosd

(十字 (2) Three phase Half wave contralled converter. (03) 3. \$ 3. pulse converter of 3-phase H-3 converter > Thurse phase M-3 converter with R Load! A E BB io At 3-\$ have tryvistor convertor feeding Rlood. -> If finding angle & is o', see TI would begin Conducting forum with 30° to 150°. T2 forom wit = 150° to 270°. T3 forom rol=270° to 390° \$ 50 on. > In other words, fouring angle for this controller convertor would be measured forom vot=38 for TI forom when 150° for T2 & from lot= 270° for T3. > Fo o° fining angle delay, thysists behaves as a diode.





(19)

> The load Inductance L is large so that load current is continuous and constant at Io:

Four floring angle 230, 16 & Vorms is same as for R-load 2000 > For firing angle trange of 30°22290° & 90°222180°, the convertor behaves differently:

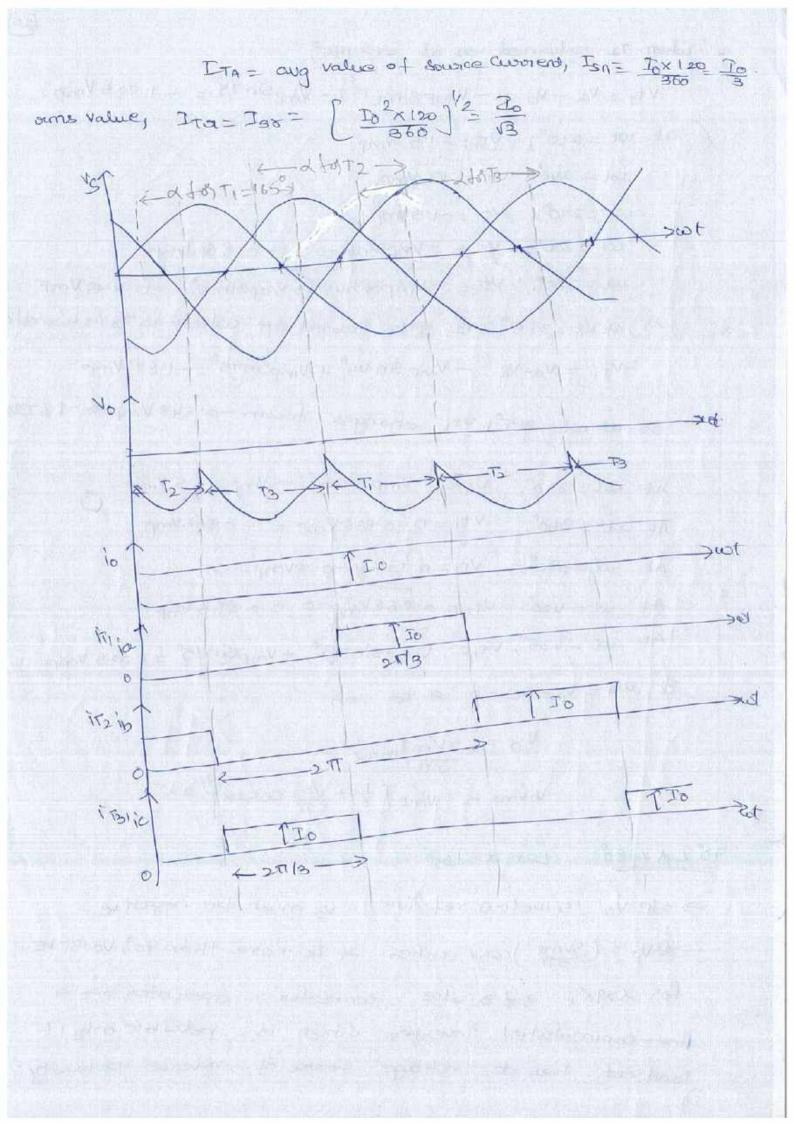
Ti conducts forum 30th to 150th, 172 conducts forum 150th to 278th, T3 forum 278th to 398th Elso on. Thus each sce conducts for 120.

At whether Va is severe but it. (Gria) is not severe because of RL load. ... Ti would continue conducting beyond whether The As such Vo = Va goes negative beyond whether suchen The is two and on at whether = 150 + x, load account shifts forem Ti to The E a voltage Va-Vb [= Vm sincisor x) forem Ti to The E a voltage Va-Vb [= Vm sincisor x) oud (to commutation.

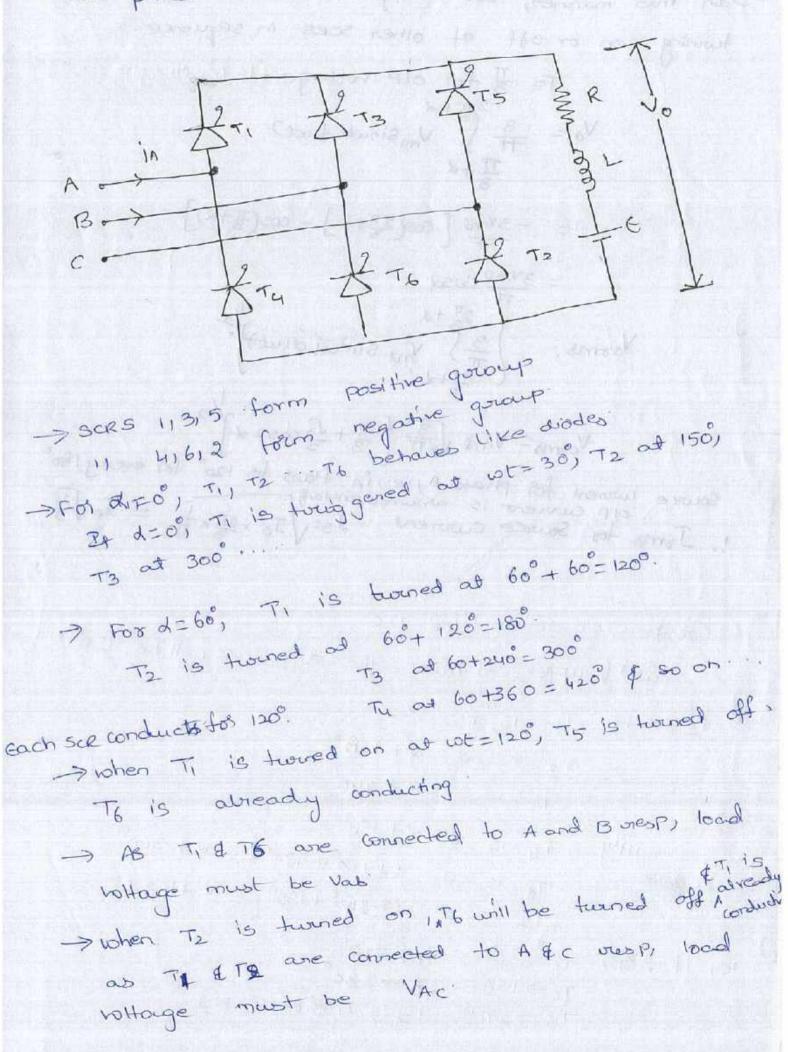
-> sce T2 conducts forom (158+x) to (270°+x) & so on

Let $d=45^\circ$. when Ti is on, $V_{T_1} = V_a - V_a = 0$ from $wt = 75^\circ$ to 19.5°. when T_2 is on, $V_{T_1} = V_a - V_b$ from $wt = 195^\circ$ to 315° and when T_2 is on, $V_{T_1} = V_a - V_b$ from $wt = 315^\circ$ to 435° ED so on.

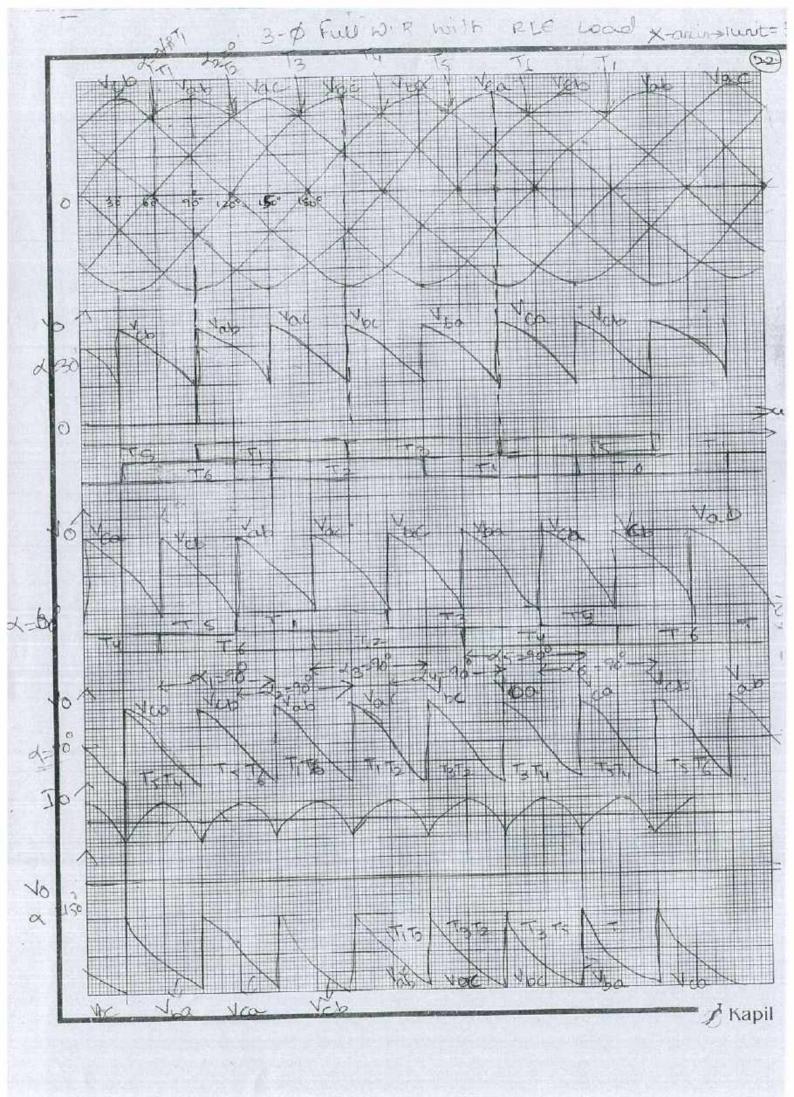
-> Solp vo is below refiline, vo must be negative. -> Solvo = (3Vmil) cosx when a is more than 90°, vois-ve. for d>90°, 3-0 3 puble converter operates as a line-commutated inverter which is possible only it load cet has de voltage source of verere polavity.

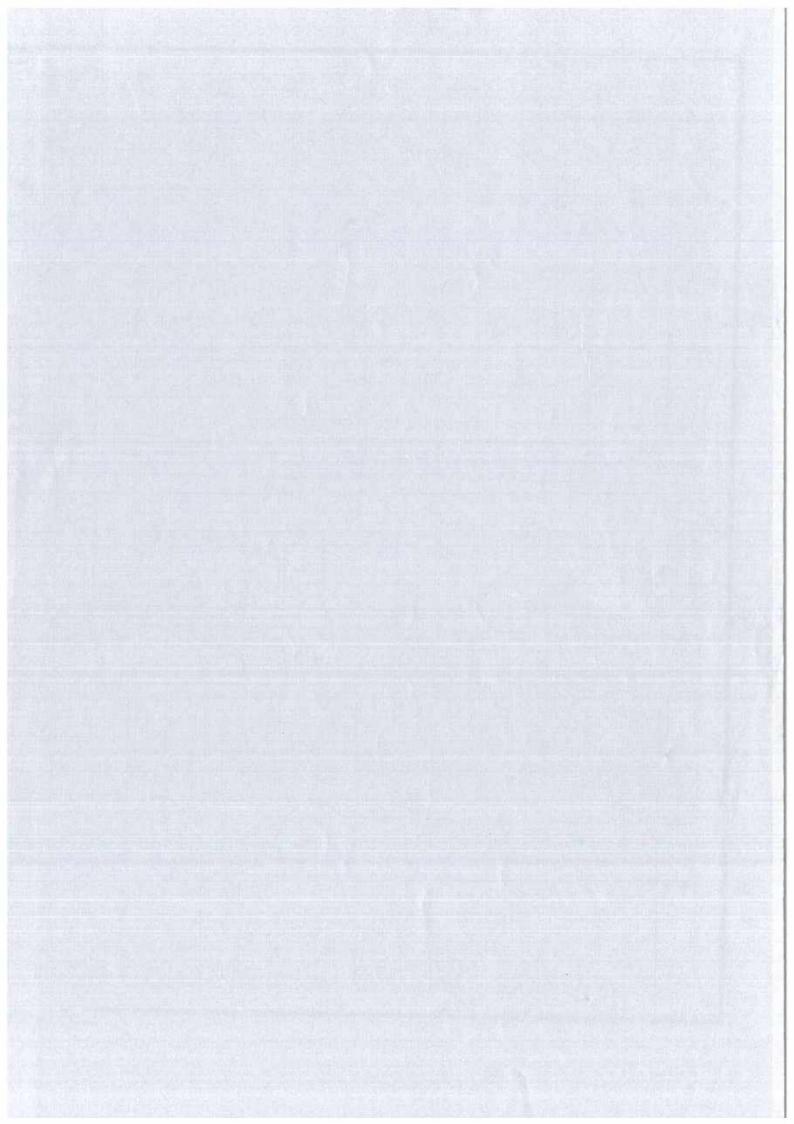


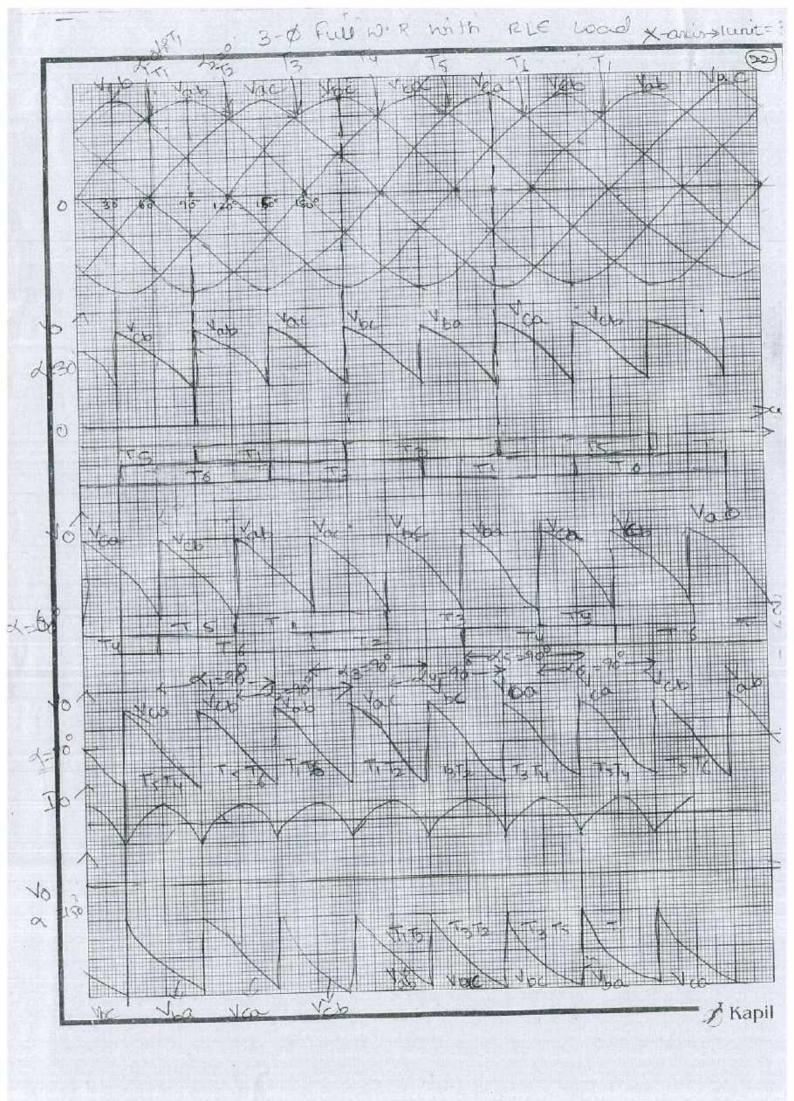
Those phase full convertor with RLE.

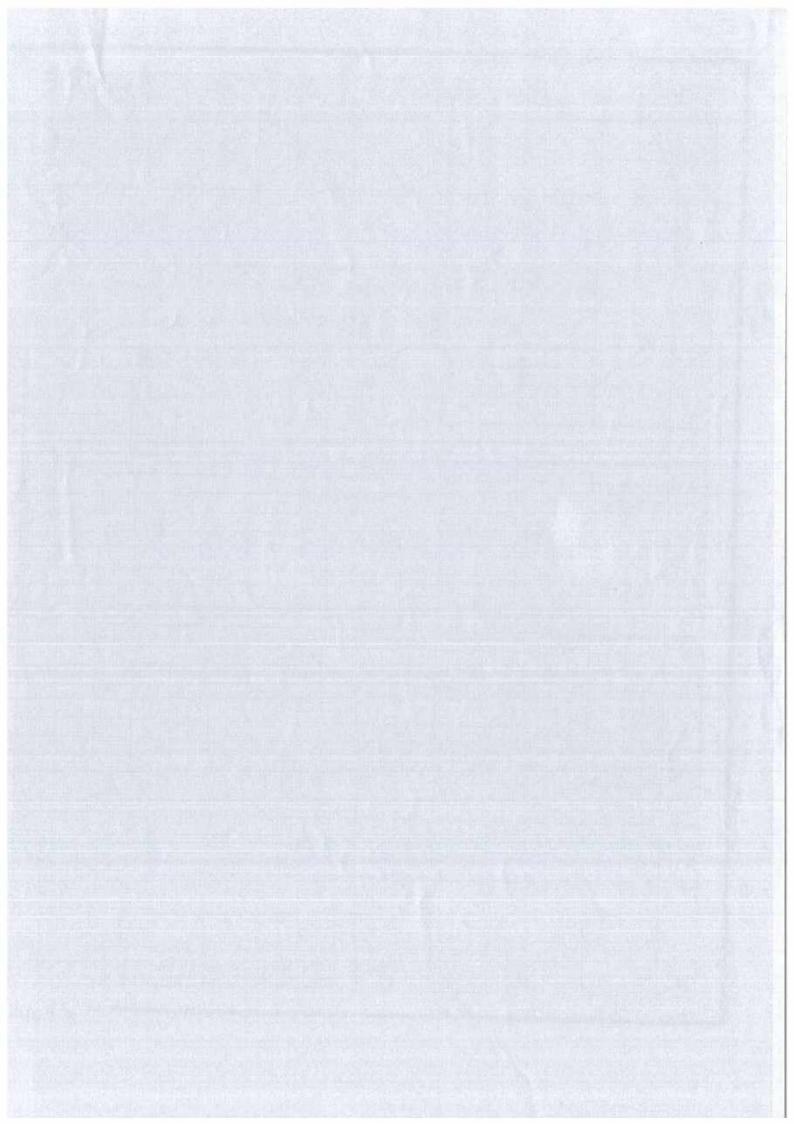


(21)





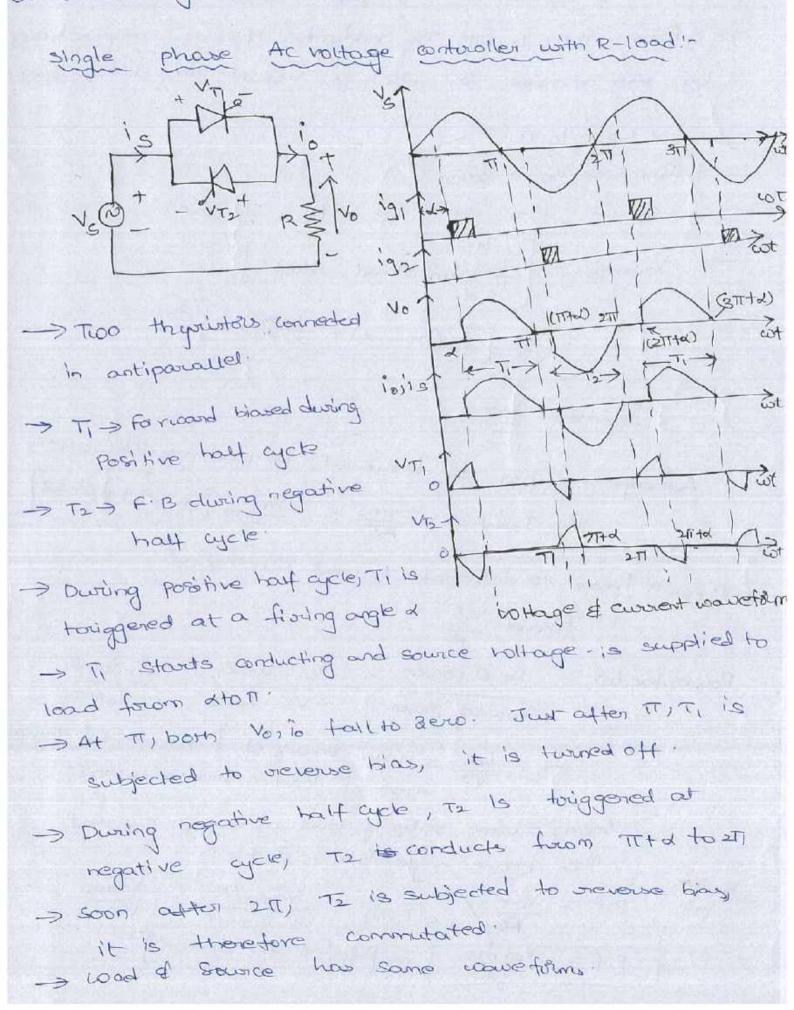




(23) Impedance Effect Source converter Full 0 For VS Tot VO yba 305 Tot 9 1000 10 II when TI & T2 are triggered, T3 & T4 I2 T 12 arready conducting " Lot KVL for toop abcd SU due to presence of LS, i 2 decureases BITY gradually to Zevie, where for TZ, Current builds up gradually from zero to full value of load curren Io u > overlap angle. During the overlap aggle 11)

UNIT-I

1-6AC voltage controllers:



0

> Form a to d, T, is forwoord blocking mode, VI, = Ks. > & VI = VS from TT to TT to TT to TT to TT to Lecause Ti is reverse bias > Form TI to to 2TT, T2 conducts, TI is :. or verse bias by VD accordes T2 which is about 1 to 1 sv (hore zero)

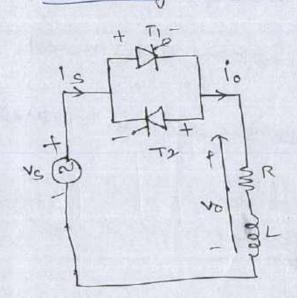
circuit two-off time
$$t_c = \frac{1}{3} \frac{sec}{\sqrt{2}}$$

Voums = $\left(\frac{1}{3} \sqrt{2} \frac{1}{2} \frac{1}{2} \sqrt{2} \frac{1}{2} \frac{1}{$

Jorms: Vor R Average power p delivered to lood resistance R's P= Jorms: Vorms = Vm² [un-1)+dsinad] P= Jorms: Pt = Vm² In R[un-1)+dsinad]

Mark power Primare its delivered to load when did

Powerfactor = Real power - Vs Ii cost, Ii cost, Apparent Power - Vs Ii cost, Iorms $I_1 = I_{1m} = urms$ value of fundamental comp- V^2 -ment of load of source current Iorms = urms value of load of source current $d_1 = \frac{1}{Var} = \frac{Var}{Vs} = \frac{Var}{Vs} R = \frac{Var}{Vs}$ $\sigma_1 = \frac{Var}{Vs} / vs Irms = \frac{Var}{Vs} R = \frac{Var}{Vs}$ $\frac{Var}{Vs} = \frac{Var}{Vs} = \frac{Var}{Vs} R = \frac{Var}{Vs}$ AC voltage controller with RL load!

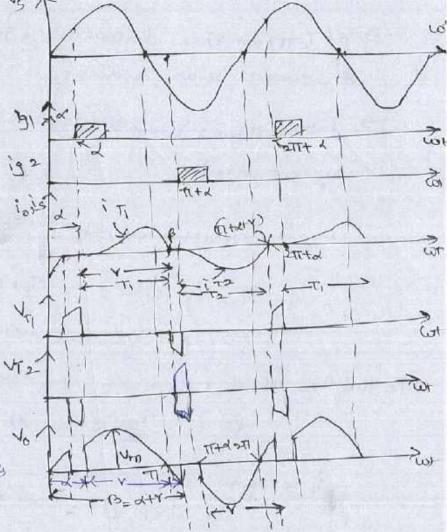


> During o to T, T, is fB At wt = a , T, is longered & is = it starts building up through load.

> At TT, load & source vottages are zero but the current is not zano because of Inductorise in load act.

-> At B>TT, load current reduces to zero p -> extinction angle

- -> After TI, TI is viewere bried but does not two off because is is not Zero. At B only when is zero.
- -> TI is have off as it is already accurse based. -) After commutation of T, at B, VinsinB appears at once as R.B.
- > From B to TIta, no cuarent exists in power direct, 1000 VTI-15,
- -> when T2 is twined on at LIT tx)7B, awarent id = iT2 stants building up in overese direction through load.



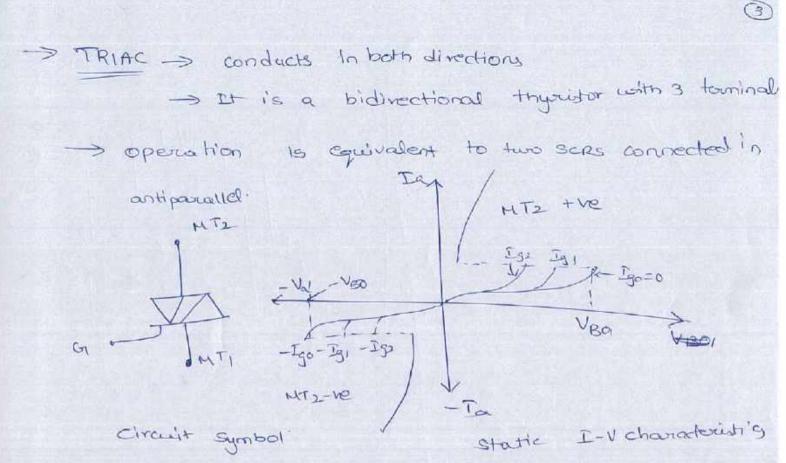
To find A, At ust = d, 10=0, t= d/10 $: io = \frac{\sqrt{22}[\sin(\omega t-\phi) - \sin(\omega t-\phi) \exp[\frac{E(\omega t-t)}{2}]}{2}$

$$\frac{Operation contraction}{P} = \frac{1}{2} \sin(B - \phi) = \sin(B - \phi) = 0.$$

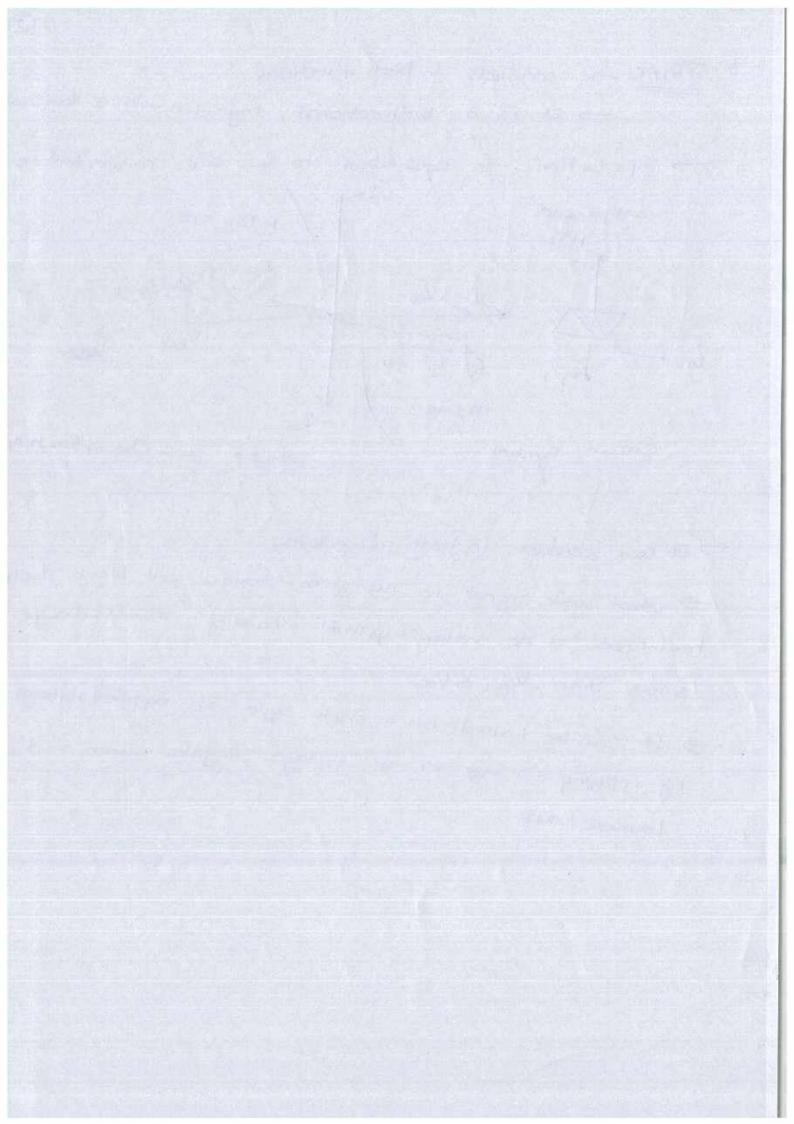
$$\oint B - d = \Pi = r$$

un de

3. If $\alpha \in \phi$ load current would not trange with α , but both scas conduct to π . τ_1 would two on α t with ϕ of τ_2 at $\pi + \phi$.



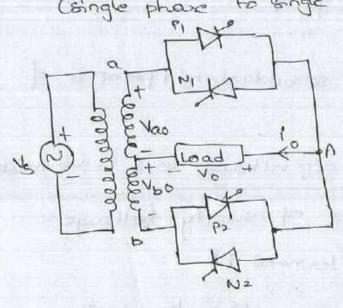
> It can conduct in both directions, -> when gate signal is not given, twiac will block both hast yere at ac voltage (applied) incase of this voltage is less than VBOI as VBOS -> It can be twened on in each cycle of applied nottage by applying a tre or -ve voltage to gale with r. t torning MTI.



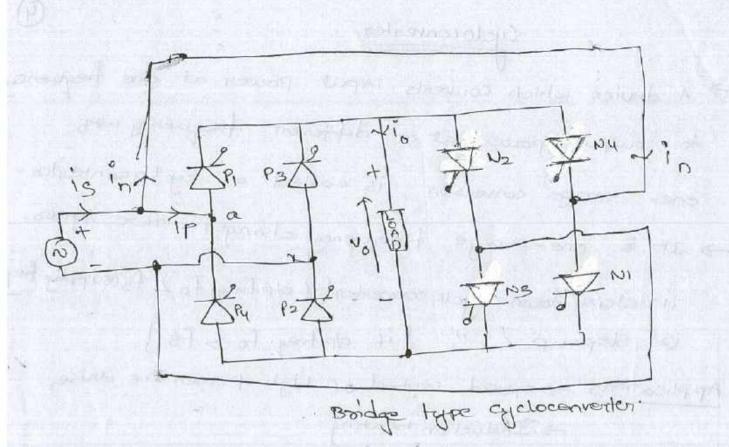
Cyclo converter

→ A device which converts input power at one frequency to output power at a different frequency with one-stage conversion is called a cycloconverterone-stage conversion is called a cycloconverteris one-stage frequency changer two types, is step-down cycloconverter (if old freq. fo 2 fs (supply feg. (2) step-up "[if old freq. fo 2 fs (supply feg. (2) step-up "[if old freq. fo > fs]] Applications → speed control of high power ac doines → Induction hearing → static VAs compensation → for converting variable speed attainates northy to constant foreg. of p variage

Pur de phase to single phase aucloconverter



Midpolot type.



1. Single phase Step-up cycloconvertiger requires forced. commutation.

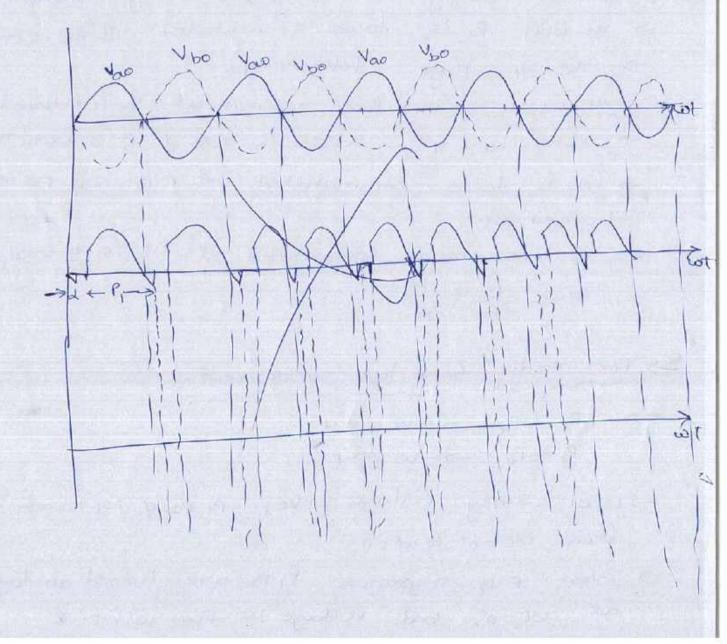
step_up cyclo converter : Mid point cycloconverter
 > P1, P2 are for positive group
 > N1 / N2 " " negative "."
 > Load is connected blue secondary mid point o el
 torminal A.

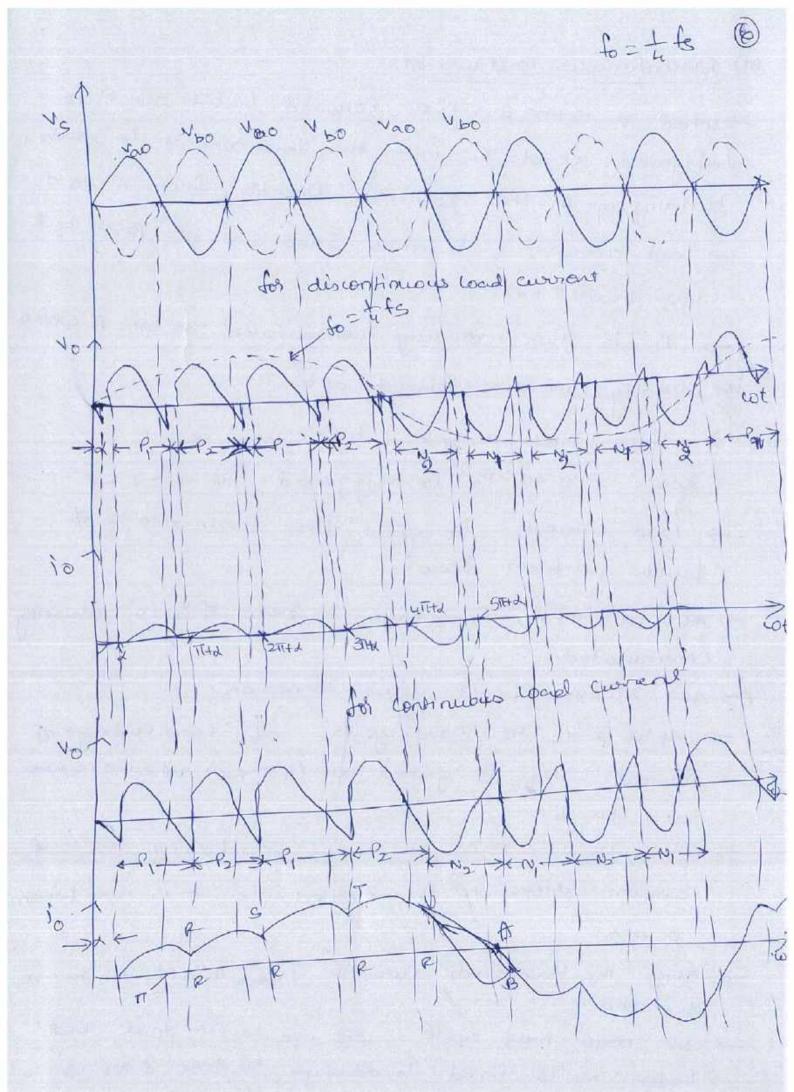
> positive directions for all roltage voltage voltage > During positive half cycle of supply toottage tourinal a is the corrit tourinal b:

->:. Pi & N2 are F.B forcom with to waterin. -> As such scr. PI is twented on at water so that load voltage is the with torminal A the p . o negative

→ At with PilB are force commutated and NO, N2 are two-ned on · with this, load voltage is -ve with terminal of two with respect to A; wad voltage tollows Noo; → At witz, N1 N2 are force commutated & Pi) P2 are two-ned on · → After witz IT, P3, Py & M3/Ny are F.B these entrefore be two-ned on & Commutated Forom witz IT 102TI.

Step-down cyclo converter! in mid point cycloconverter!





(a) Alscontinuous load aurient:

-> when a listle wort. o, forward biased see P, is toriggevied at ust= x, with this load current 's starts building up in the positive direction from A to 0. -> load avvient & becomes zero at lot B717 bud less than(IT+d).

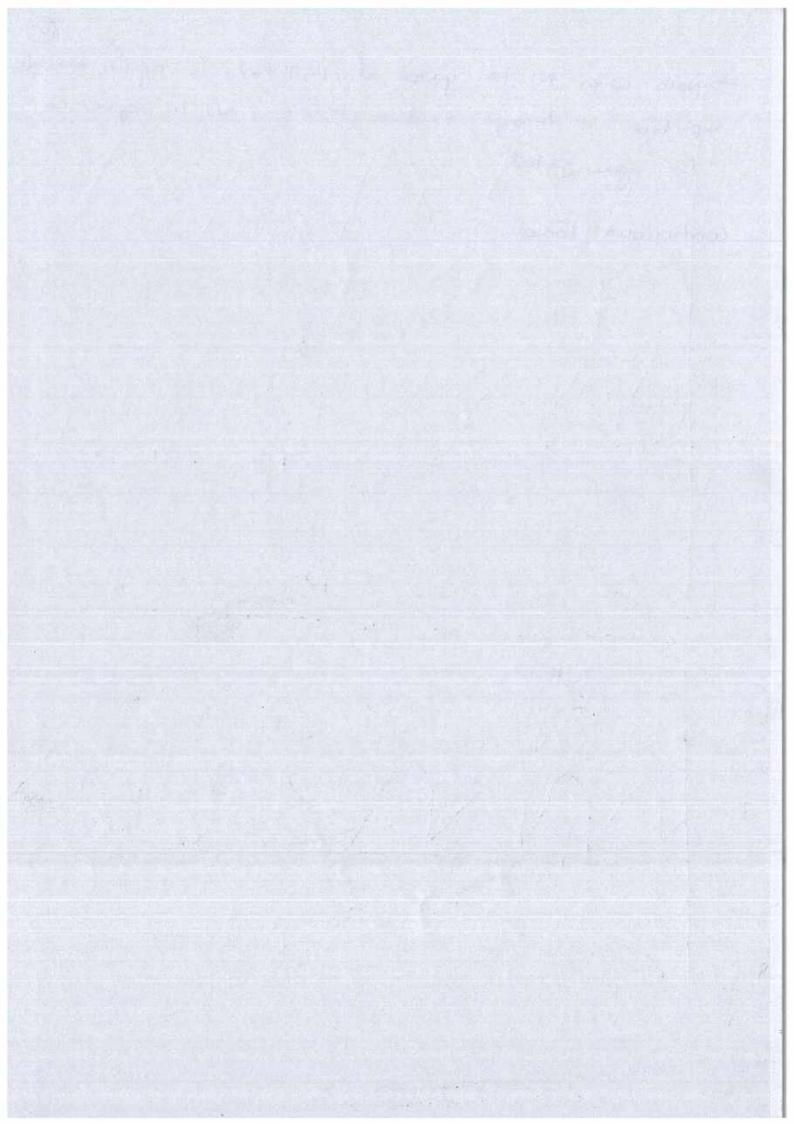
- -> P1 is thus naturally commutated at cot= B which is already viewerse biased after TT.
- -> After half a cycle, bis the wort o > NOW FIBSER P2 is triggered at lot= T+x. > Load current is again the foram Ato of builds up forom Zeno.
- > AI LOT = TITB, lo de cays to dero \$ 12 is naturally Commutated.
- > At 211+x, Pi is again turned on. -> After 4 the half cycles of loadholtage of airrent, N2 is gated at (4TT+a) when oistre w.r.to

6.

- -> As No Is FIB it starts conducting but load auvent direction is neversed, ie, it is now forom o to A.
- -> After N2 briggered, Curvient flows builds up in-re divection.
- -> In nout half cycle ois the work to a but before will is fired to decays to serve & N2 is Commuta ted naturally

> Now when NI is gated at (517+2), is again builds up but it decays to some before N2 in sequence is againgated.

continuous load



tion volt Load volt ion tott ion tottt ion tottt ion tottt ion tottt ion tottt ion tottt stepdownchopper cordiciaes A & Type A O chopper O Pt SW I TOOD mode I when sw is closed, ie, during Ton, choppen is on & load ~voltage is equal to -> During twinoff Intowal Tott, chopper is oft, load current flows twough freewheeling diode FD -> As a result, load terminals are short circuited by FD and Load voltage is therefore zero during > In this manner, the chopped dc Whage is publiced at the load terminals. -> During Ton, load correct vises othereas during Tys, load current decoups Average voltage Vo = <u>Ton</u> Vs = <u>Ton</u> v = alls Tont Tolt d = Ton > duty cle " Vo=f. Ton'Vs T= Tont Totf = chepping period f=f=chopping frequency

control strategies.

The owerage voltage of old, vo can be controlled through a by opening and closing the semiconductor Switch periodically -> The Various control strategies for varying duty cycle & are as follows 1. Time viatio Control (TRC)

2. avoient - l'imit contorol.

1- Time viatio contocol (TRC)

-> Time viatio Ton is varied. -> this his realized in two different structegies called constant forequency system Quarcable forequency System :

(i) constant forequency system:

> The on-time Ton is varied but chopping forequency f (or chopping period T) is kept constant. Varion of Ton means adjustment of pulse width, as such this scheme is also called pube-width modulation $\tau \rightarrow 0$ to 1 $V_0 \rightarrow 0$ to V_0

(ii') Variable forequency system: -> The chopping forequency f (or chopping period is kept constant variation = is varied and either (i) on-time Ton is kept constant of (ii) off-time Topp is kept constant" (iii) off-time Topp is kept constant" modulation

lof - Tomar current_limit control. > The on & off of chopper circuit Tomin guided by the purevious set E-TON-KE-TOFF value of load awarent -> These two set values are more. load current Ioman & minimum Vo Load current Iomin S when load current preaches the IVS upper limit Iomax, chopper is current - litrit Conturol and begins choppent Switched off.) Now load awarent foreewheels - when it falls to lower limit Formin, chopper, to decay exponentially is suritched on & load autorent begins to suise Steady state time domain analysis of stepdown chopper THE FOR THE TOTAL mode (ii) ig FIT I Imin 1 7 ony the equivalent is iot Inter shown in fig. 0 sts Ton. vs TT Vá No= Ri+Ldi+e. >0 KENT-A mode(ii) when switch is off, for continuous aurent 0= Rit Ldite

Applying Laplace towas town to
$$e_{p} O$$
, interfacement - Inin

$$\frac{V_{S-e}}{s} = RT(S) + L(ST(S) - Imin)$$

$$\Rightarrow T(S) = \frac{V_{S-e}}{s} = L(S) [R + LS] - LTmin$$

$$\Rightarrow T(S) = \frac{V_{S-e}}{s} = L(S) [R + LS] - LTmin$$

$$\Rightarrow T(S) = \frac{V_{S-e}}{s(R+LS)} + \frac{LTmin}{(R+LS)}$$

$$T(S) = \frac{V_{S-e}}{LS[S+R]} + \frac{LTmin}{V(S+R]}$$

$$T(S) = \frac{V_{S-e}}{LS[S+R]} + \frac{LTmin}{V(S+R]}$$

$$T(S) = \frac{V_{S-e}}{LS[S+R]} + \frac{Tmin}{V(S+R]}$$

$$Touching inverse Leptace to above equation /
$$i(t) = \frac{V_{S-e}(1 - e^{R_{T}t}) + Tmine^{-\frac{R_{T}t}{T}} = 3$$

$$Applying Laplace - bians from to eq. (2) initial access = 2max$$

$$-\frac{e}{S} = R(T(S) + L(ST(S) - Tmax)$$

$$\Rightarrow T(S) = \frac{e}{P(1 - e^{-\frac{R_{T}t}{T}})} + Tmine^{-\frac{R_{T}t}{T}} = 3$$$$

tor lon 2 t = 1; when t= Ton; t'= 0 where t'= t-Ton; when t= T; t'= T-Ton= Toff

eq (5) at t= Ton,
$$i(t) = I \max -\frac{Ton}{Ta}$$

 $\Rightarrow I \max = \frac{V_{s-e}}{R} \left[1 - e^{\frac{Ton}{Ta}} \right] + I \min e^{\frac{Ta}{Ta}}$
 $iotor Ta = \frac{L}{R}$

$$\begin{array}{cccc} & @ & at t' = \operatorname{Tot} f = \operatorname{T-Ton}, & i(t') = \operatorname{Imin} & -\left(\frac{T-\operatorname{Ton}}{Ta}\right) & -\left($$

Sub
$$eq. (i)$$
 in $eq. (i)$

$$Inon = \frac{V_{S}-E}{12} \left[1-e^{-\frac{Ton}{Ta}}\right] + \left[-\frac{E}{2}(1-e^{-\frac{Ton}{Ta}}) + \frac{Ton}{Ta}\right] + \frac{Ton}{Ta}$$

$$\Rightarrow I_{max} = \frac{V_{S}}{R} \left[\frac{1-e^{-T_{A}}}{1-e^{T_{A}}} \right] - \frac{e}{R} \longrightarrow \textcircled{P}$$

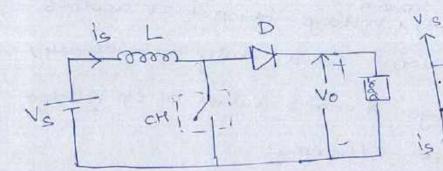
I'lly
$$e_{q} \otimes ine_{q} \otimes i$$

 $Imin = \frac{V_{s}}{R} \begin{bmatrix} 1 - e^{\frac{T}{Ta}} \\ 1 - e^{\frac{T}{Ta}} \end{bmatrix} \frac{e^{\frac{T}{Ta}}}{e^{\frac{T}{Ta}} - \frac{G}{R}}$
 $Imin = \frac{V_{s}}{R} \begin{bmatrix} \frac{e^{\frac{T}{Ta}}}{1 - e^{\frac{T}{Ta}}} \end{bmatrix} - \frac{E}{R} = \frac{1}{R}$
 $In case cH conducts continuously then $Ton = T$
for on eqns $\bigoplus a e_{q} \otimes \frac{1}{R}$
 $Imox = Imin = \frac{V_{s} - e}{R}$$

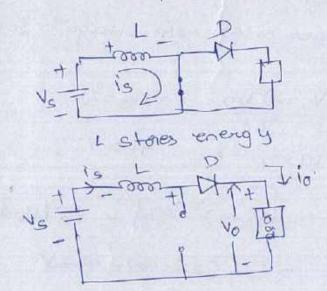
Stady state vinnle

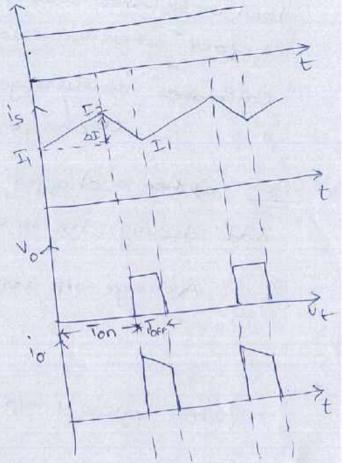
$$\Rightarrow$$
 the current pulsates the Imax & Enin
 \Rightarrow the vinnle current (Emax - Enin) (on be obtained
for $\textcircled{P} \textcircled{P} \textcircled{P}$
Inor Imin = $\frac{V_{S}}{P} \left[\underbrace{1 - e^{-\frac{T_{R}}{T_{R}}}}_{1 - e^{-\frac{T_{R}}{T_{R}}}} - \frac{e^{\frac{T_{R}}{T_{R}}}}{e^{-\frac{T_{R}}{T_{R}}}} \right]$
 $= \frac{V_{S}}{P} \left[\underbrace{1 - e^{-\frac{T_{R}}{T_{R}}}}_{1 - e^{-\frac{T_{R}}{T_{R}}}} - \underbrace{(1 - e^{-\frac{T_{R}}{T_{R}}})}_{1 - e^{-\frac{T_{R}}{T_{R}}}} \right]$
 $= \frac{V_{S}}{P} \left[\underbrace{1 - e^{-\frac{T_{R}}{T_{R}}}}_{1 - e^{-\frac{T_{R}}{T_{R}}}} - \underbrace{(1 - e^{-\frac{T_{R}}{T_{R}}})}_{1 - e^{-\frac{T_{R}}{T_{R}}}} \right]$
 $= \frac{V_{S}}{P} \left[\underbrace{(1 - e^{-\frac{T_{R}}{T_{R}}})}_{1 - e^{-\frac{T_{R}}{T_{R}}}} - \underbrace{(1 - e^{-\frac{T_{R}}{T_{R}}})}_{1 - e^{-\frac{T_{R}}{T_{R}}}} \right]$
 $= \frac{V_{S}}{P} \left[\underbrace{(1 - e^{-\frac{T_{R}}{T_{R}}})}_{1 - e^{-\frac{T_{R}}{T_{R}}}} - \underbrace{(1 - e^{-\frac{T_{R}}{T_{R}}})}_{1 - e^{-\frac{T_{R}}{T_{R}}}} \right]$
 $= \frac{V_{S}}{P} \left[\underbrace{(1 - e^{-\frac{T_{R}}{T_{R}}})}_{1 - e^{-\frac{T_{R}}{T_{R}}}} - \underbrace{(1 - e^{-\frac{T_{R}}{T_{R}}})}_{1 - e^{-\frac{T_{R}}{T_{R}}}} \right]$

The vinite avoient is many that is $\frac{1}{1-e^{-\frac{1}{2}}}$ unith $Ton = \alpha T$ $\theta T - Ton = (1 - \alpha)T_{j}$ $\frac{1}{1-e^{-\frac{1}{2}}}$ $\frac{1}{1-e^{-\frac{1}{2}}}$ Step-up choppen:



skpup chopron





$$= V_{S} \left[\frac{T_{1} + T_{2}}{T_{2}} \right] \overline{V}_{O}$$
when $\overline{V}_{O} + \overline{V}_{1}$ = $V_{O} + V_{S} = V_{S} \left[\frac{T_{1} + T_{2}}{T_{2}} \right] \overline{V}_{O} + \overline{V}_{S}$

$$V_{S} \left[\frac{T_{1} + T_{2}}{T_{2}} \right] \overline{V}_{O} + \frac{T_{1} + T_{2}}{T_{2}} \right] \overline{V}_{O} + \frac{T_{1} + T_{2}}{T_{2}} \overline{V}_{O} + \frac{T_{1} + T_{2}}{T_{2}} \overline{V}_{O} + \frac{T_{1} + T_{2}}{T_{2}} \right] \overline{V}_{O} + \frac{T_{1} + T_{2}}{T_{2}} \overline{V}_{O} + \frac{T_{1} + T_{2}}{$$

O

Soll-a)when a chopper is on, old voltage is (Vs-2) tolks and during the time chopper is off; old voltage is zero

: Average of P voltage:
$$(V_{0}-2)T_{0} = q(V_{0}-2)$$

= $q(V_{0}-2) = q(V_{0}-2)$

Rims value of old voltage =
$$(V_{5}-2)^{2} \overline{D_{7}}^{2} = V\overline{a}(V_{5}-2)^{2}$$

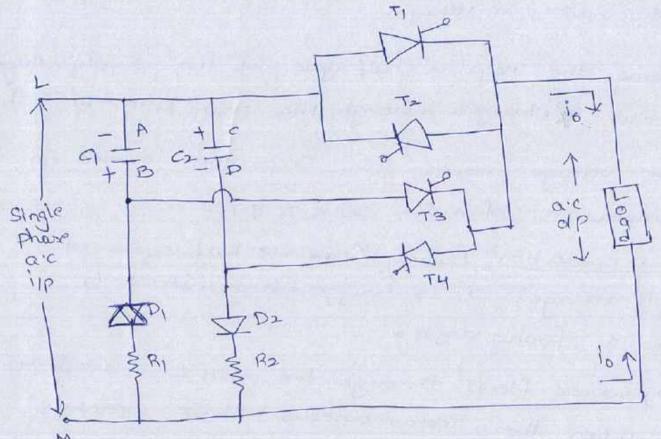
= $V_{5} \overline{L}(230-2) = \frac{1}{2} \frac{1}{2}$

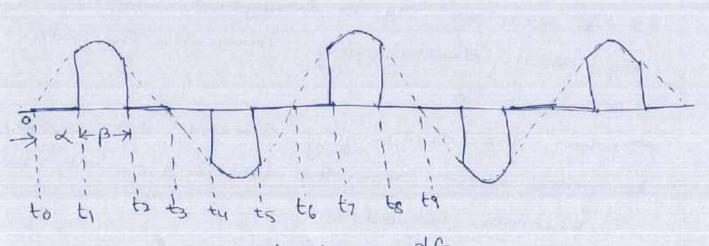
(b) power of p or power delivered to body

$$P_0 = \frac{V_0^2 r}{12} = \frac{(144 \cdot 2)^2}{10} = 2079 \cdot 364 \text{ km}$$
Power if p to chopper $P_1 = V_5 E_0 = 2.30 \times \frac{91 \cdot 2}{10} = 20976 \text{ km}$
Chopper efficiency = $\frac{P_0}{P_1} = \frac{99 \cdot 13.90}{10}$

<u>Ac chopper</u> - vollage changing àrcuits employing servicenductor devices as a static switch are known as a.c. chopper-

5





Load voltage ulf

-> TI & T2 are main SCR T3 & T4 are auxiliary SCRS C1 & C2 are commutating Capacitals. D1 & D2 provide changing path of for the Capacitals Thysuistons Ti and T3 tooms the first pair for producing the positive alternation, and Tag Ty constitute the second pair four producing the negative alternation of the input according.

> During the negative half agele of the supply hollage capa dits changes thorough the path M-RI-DI-CI-L > The voltage across these Capacitos is used (to) commutation of main Scess T, & T2' unde 1 openation: buring 1st positive half cycle of Supply toltage, T1 is truggered at instance to with a firsting angle & -> current flows thorough the path L-T1-bood-M. -> when the instantaneous voltage treaches

the instant T2, auxiliary thyrists T3 is truggered. > As soon as T3 is truggered, Capacitosci while start discharging through the path CB-T3-T1-CA:

The comes more than the forward current, SCR Tip The comes twined att.

-> auxiliary T3 will be automatically homed off at instant t3 because of the serie current at this instant. -> Hence, scrs T1 & T3 forms the first pair for producing the positive altomation of ilp accrollage

Mode 11 operation For the formation of the negative alternation, second pair of thyristons I of Ty are used -> Main SCR T2 is touggered at the instant the during - first negative hast-cycle of ilp voltage. -> The current flows through the path M-load-5-1 -> when the Instantaneous witage reaches the instant ts, sar Ty is triggered. -> As soon as thysister Th is tunggened , capalit

S AS Soon us myclishes in the south C2 will start discharging through the path C2 - T2 - T4LA-KI - CD.

→ when this discharging arrent is more than the load arrent, see To becomes turned off. → At instant to, see Ty is automatically traned off as the arrent passing through it becomes zero → Again at instant to, see Ti is toriggered to produce the new next positive alternation

> The load power can be changed simply by Varying the public - width for conduction angle) B

> The fundamental ilp pit is always unity > This cut is generally used for obtaining a regulated air old rollage

6

$$V_0 = V_0 \cdot \frac{1}{1-d}$$

=> 660 = 220 $\frac{1}{1-d}$ => $d = \frac{2}{3} = \frac{T_{00}}{T}$.

Ton:
$$\frac{1}{3}T = 100 \text{ MS}$$
.
i. chopping period T: $100\times\frac{3}{3} = 150 \text{ MS}$.
pube width of diprottage=Toff= T-Ton
=150-100 = 50 \text{ MS}

Toff=
$$\frac{50}{2} = 25 \text{ MS}^2$$

For constraint frequency operation, $T=130 \text{ MS}$
Ton= $150 - 25 = 125$
MS

$$x = \frac{T_{00}}{T} = \frac{125}{150} = \frac{5}{6}$$

$$\therefore V_0 = 220 \times \frac{1}{1 - \frac{5}{6}} = \frac{1320 V'}{1 - \frac{5}{6}}$$

When C.H., is turned OFF, the load current follows the source pulli by reversing the polarities of the inductor through the conducting should D.. The load current path when chopper C.H., is in turned OFF state is

$$L = E - CH_4 - D_2 - L$$

For the second quadrant operation chopper CH₂ is operated while $\mathrm{CH}_{\mathrm{tr}},\mathrm{CH}_{\mathrm{sh}}$

 CH_4 are in the OFF state. Here, $E > \frac{Ldi}{dt}$, hence reverse correct flows whenever

 OH_2 is in the on state. It's path may be given as

$$F^* - L - CH_2 - D_4 - E$$

During this period, the inductor gets charged. When CH₂ is in the OFF state, the load current flows in the same direction by following the path as shown.

$$L^{*} = D_{1} = E_{dc}^{*} = E_{dc}^{*} = D_{4} = E = L^{*}$$

In this second Quadrant operation of chopper, power is fed back from load to

ource as the voltage
$$E + \frac{Lat}{dt} > E_{dc}$$

For third Quadrant operation, chopper CH₃ is operated while CH₁. CH₄ are in the OFF state and CH₂ is in the ON state. In order to operate the chopper in this quadrant, the polarity of E must be changed. When CH₁ is in the on state the load voltage is negative and the load current is also negative whose path may be given as follows:

$$_{1c}^{+} - CH_3 - E - L - CH_2 - E_{dc}^{-}$$

When CH_a is turned off, the load current follows the path as shown below through CH_2 and diode D_4 .

$$L^{+} - CH_{2} - D_{4} - I$$

For fourth quadrant operation, chopper CH_4 is operated by keeping the other choppers in the OFF state. Here also, the chopper operates only when polarity of E is reversed. The load current follows the path as shown.

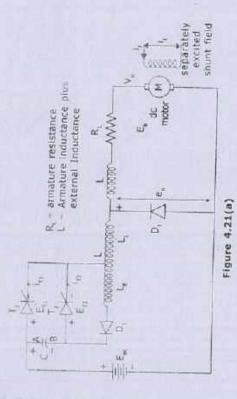
$$^{+}$$
 - CH₄ - D, - L - E

The current direction is positive, whereas load voltage is negative whenever CH₄ gets turned OFF, and the load current follows the path as shown by conducting diods D₂ and D₃.

$$L^{*} - E - D_{3} - E_{dc}^{+} - E_{dc}^{-} - D_{2} - L^{-}$$

Here also, the power is fed back to source from load

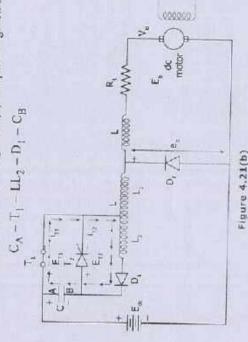




Circuit description

Inconsists of main thyristor T_1 , auxiliary thyristor T_2 . Commutating circuit for main thyristor consists of capacitor C, diode D₁, T₂, autotransformer. The main definiting of using autotransformer is that, it eliminates the commutation failure, since the energy stored in LL₂ slightly enhances the capacitor voltage to a value grater than E_{db} from which the definite commutation process occur as L₁ and L₂ are closely coupled. In this chopper, type, 'D' commutation process occurs corris. The operating principle may be explained in different modes

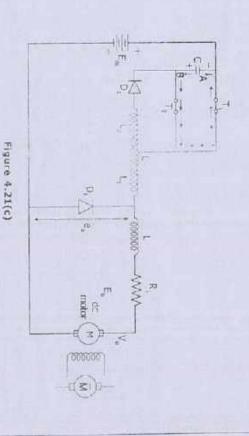
Node 1: Initially, the capacitor 'C' is assumed to be charged to a voltage E_{dc} with the polarity as shown. When SCR T_1 is triggered at the instant $t = t_a$, the arrent follows the path as shown in fig. 4.21(b). Its path is given as



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Now, the capacitor $(1, \dots, n)$ harged to the opposite polarity i.e., plate g becomes positive and plane (3, n) becomes negative. Diode D_1 prevents further oscillation of L_2C circuit. Thus, suparitor retains its charge till the thyristor T_1 gets triggered. When the thyristor L_1 is in the on-state for a long duration of time then the motor reaches the steady state speed determined by the battery voltage, the motor and the mechanical load characteristics.

Mode 2: At the instant $t=t_c$ SC R T_2 is turned on Now, the current follows the path as shown in Fig. 4.21(c)



Its path is given as,

$$C_B - T_2 - T_1 - C_A$$

Hence, the capacitor discharge reverse biases the thyristor T_1 and it gets turned off. Whenever capacitor C^* is recharged, SCR T_2 gets turned off because the current through it fails below that of the holding current value. When SCR does not conduct, inductance L-maintains the load current through diode $D_{\rm fb}$. Thus, the motor torque proportional to load current becomes smooth instead of pulsating in nature. At the instant $t = t_{\rm c}$, bottom plate of capacitor C^* reaches a peak value greater than $E_{\rm dc}$. The time duration $t_{\rm c}$ to $t_{\rm d}$ is known as circuit turn off time.

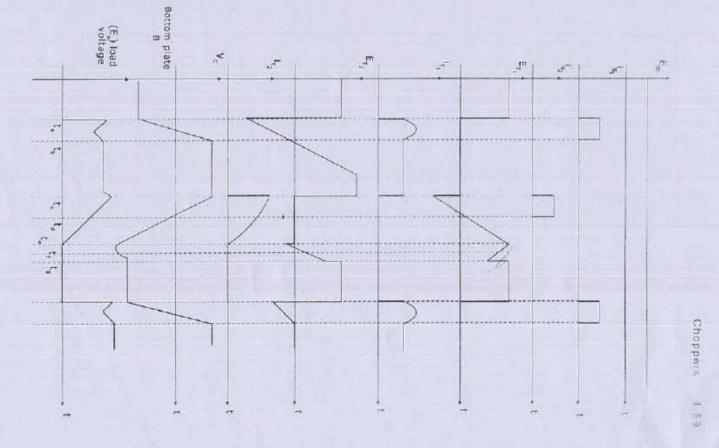


Figure 4.21(d) Voltage and current waveforms in D.C Jones Chopper

Hower Electronics 4.60

Design consideration

for the design of Jones chopper circuit. Initially, maximum current longy flows Proper selection of committating capacitor 'C' and auto transformer 'T' is essential through L1. During the turn off time of SCR T1, the energy stored in inductance L₁ is transferred to capacitor 'C'

Hence,
$$\frac{1}{2}$$
 L₁ l²_{curax} = $\frac{1}{2}$ C V_c²
or $\frac{\sqrt{c}}{l_{omax}^2}$ = $\frac{L_1}{C}$

or
$$V_c = I_{omax} \sqrt{\frac{U_1}{C}}$$

During turn off time of the SCR,

$$t_q = \frac{v_{a}x_{b}}{I_{omax}}$$

By substituting the value of Ve in the above equation, we get

$$t_q = \frac{I_{omax} \sqrt{L_1} c}{I_{omax}}$$
$$= \sqrt{L_1 c}$$

Dividing Equation (1) by Edu results

$$\frac{V_{c}}{E_{dc}} = \frac{I_{omax}}{E_{dc}} \sqrt{\frac{L_{1}}{C}}$$

Let us assume,

$$\frac{V_c}{\Gamma_{dc}} = g; \quad R_m = \frac{E_{dc}}{\Gamma_{ormax}}$$

By substituting these values in equation (2), we get

$$\mathbf{g} = \frac{1}{R_{\rm m}} \sqrt{\frac{L_{\rm f}}{C}}$$

Voltage across SCRs T₁ and T₂ may be given as $V_c = g.E_{clo}$

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Thus, as the value of g increases, the requirements of increase in voltage rating of SCR results. Efficiency of circuit: As dissipative elements used in this chopper circuit are winding resistance and forward conducting resistance of SCRs and diodes the efficiency of the circuit increases.

Problem 12

main SCR is 100 Amps, conductance = 4mho. Calculate the value of the The Jones chapper controls the speed of separately excited dc motor. If the ip voltage $E_{dc} = 60$ v, turnoff time = 10 μ sec and the current flowing through commutating capacitor C and transformer inductances L_1 and L_2 for the

Solution: Given

Ξ

given data

turn off time
$$(t_q) = 10 \ \mu \text{ sec.}$$

 $t_0 = 1_{T1} = 100 \text{ A}$
 $g = 4 \ mho$
 $g = \frac{1}{R_m} \sqrt{\frac{L_q}{C}}$
 $R_m = \frac{L_{qc}}{t_0} = \frac{60}{100} = 0.6\Omega$
 $\sqrt{\frac{L_q}{C}} = 4(0.6) = 2.4$

But we know that,

(5)

or

Ð

5

(1) and (2)
$$t_q = \sqrt{L_1 C} \text{ or } \sqrt{L_1 C} = 10 \times 10^{-6}$$

$$\sqrt{\frac{L_1}{C}} \sqrt{L_1C} = (2.4) \ 10 \times 10^{-6}$$

$$L_1 = 24 \times 10^{-6} = 24 \mu I$$

itute L_1 value in equation (2) gives

 $24 \times 10^{-6} \times C = (10)^2 \times (10^{-6})^2$

 $\sqrt{24\times |0^{-6}|} \times \sqrt{C} = 10\times 10^{-6}$

$$I_{\rm el} = 24 \times 10^{-6} = 24 \mu H$$

$$L_1 = 24 \times 10^{-6} = 24 \mu H$$

$$L_{1} = 24 \times 10^{-6} = 24 \mu L$$

$$L_1 = 24 \times 10^{-6} = 24$$

$$L_1 = 24 \times 10^{-6} = 1$$

$$L_1 = 24 \times 10^{-6}$$

Substutitute L, value in equation (2)

$$I_{1} = 24 \times 10^{-6} = 24$$

$$L_1 = 24 \times 10^{-6} = 24$$

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 $C = \frac{100 \times 10^{-12}}{24 \times 10^{-6}} = 4.16 \, \mu F$

 $L_1 = L_2$ $L_2 = 24 \mu H$

4.15 MORGAN CHOPPER

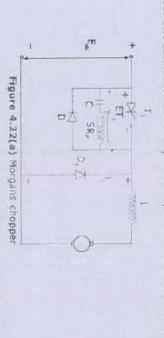
Circuit description

Morgan chopper consists of one S.C.R known as main thyristor. The advantage of using this circuit is, the cost is very low because of the presence of single SCR. The commutating elements in this circuit are capacitor 'C', saturable Reactor (SR), and diode (D). There exists a difference between air core inductor and saturable reactor.



As air can take any amount of flux, the aircore inductor never saturates. The inductance offered by the air core inductor is very large. In the case of S.R. it can saturate for a low value of exciting current. The inductance offered by the S.R is very low.

Mode 0: (Charging of the capacitor). When the S.C.R T_1 is in OFF state, the capacitor 'C' will charge to the supply voltage (E_{d_c}). The charging path will be $E_{d_c+} - C_+ - C_- - SR - L - Load - E_{d_c-}$ as shown in Fig. 4.22(a). The inductance offered by the S.R is very low. When the capacitor charges to E_{d_c} , the charging will be stopped. The saturable reactor is placed in positive saturation condition.



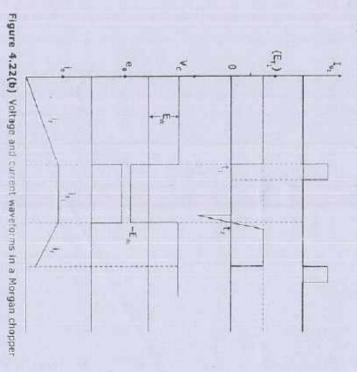
Mode 1: Give the gate signal to the chopper at the instant $t = t_1$. When the chopper is turned ON, the voltage across the capacitor is applied to the saturable reactor. The core flux direction is driven from positive saturation to negative saturation. When the S.R changes completely from positive saturation to the

negative saturation. The capacitor |U| discharges through the path. (C₁ = S C R (T₁) - S.R - C₂). LC circuit forms a resonating circuit with a discharging time of

 $T_{\rm IV}L_{\rm S}C$ see where $L_{\rm S}$ is the post saturation reactance. Since the discharging time is very small, the capacitor 'C' will reverse the charge very quickly. The capacitor voltage $-E_{\rm de}$, is applied on the saturable reactor in the reverse direction. The core is driven from negative saturation towards positive saturation. After some time, the core flux reaches the positive saturation, the capacitor will discharge the charge in opposite direction to the Main S.C.R. (T₁). So the S.C.R. (T₁) is urned off.

Mode 2: The free wheeling Diode (D_f) jets forward biased because of the stored energy in the inductor. The load current flows but the Load output voltage is zero.

The time required to saturate the core is constant which depends on the volt-time integral. The conduction period for the S.C.R is fixed, and is function of the L_s and 'C'. The average output voltage can be altered by changing the operating frequency. The total entine for the S.C.R ($T_{\rm f}$) is determined by the time required for the reactor to move from positive saturation to the negative saturation and back to positive saturation only. The associated Waveforms of morgan's chopper is as shown in Fig. 4.22(b)



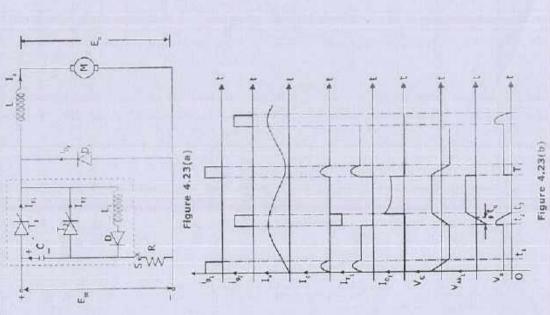
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4,46 OSCILLATION CHOPPER

Oscillation chopper is also known as Benningin's choppen.

Circuit description: Its circuit diagram is as shown in Fig. 4.23(a).

It consists of a main thyristor T_1 . The commutating circuit elements of thyristor T_1 are the auxiliary thyristor T_2 , equator C' inductor L_1 and diode D. At the time of charging, the capacitor C', resistor R' is placed in series with the switch which are connected across the dc supply. It consists of a freewheeling diode D_f . Its operation may be explained in different modes as follows:



Choppers 4.65

Mode 1: During this mode, the capacitor 'C' gets charged to a voltage of E_{de} by closing the switch 'S'. It's charging path may be given as

whenever the capacitor gets charged to a voltage of E_{dc} with upper plate positive and lower plate negative as shown in Figure, current through the resistance is zero. Hence, the switch "S" may be opened

Mode 2: Whenever thyristor 'T₁' is triggered, it comes into the conduction state from forward blocking state. During this mode, two currents flow through the thyristor T₁. One is the load current (I₀), and the other is the capacitor discharging current (I₀). Load current path may be given as

$$E_{de}^{+} = T_1 = L = load = E_{de}^{-}$$

capacitor discharging current (Io) follows the path as shown

$$C^{\dagger} - T_{1} - L_{1} - D - C^{\dagger}$$

Mode 3: During this mode, the capacitor 'C' gets charged with the reverse polarity i.e., with lower plate positive and upper plate negative. Now, the auxiliary thyristor 'T₂' gets into the forward biased condition. *Mode 4*: During this mode, auxiliary thyristor T_2 is triggered in order to commutate the main thyristor T_1^+ . As the thyristor T_2^+ gets into the forward biased condition, as seen in the previous mode it gets into the conduction state when it is triggered. Now, the capacitor discharging current flows through the auxiliary thyristor (T_2) . It's path may be given as

$$C^{+} - T_{2} - T_{1} - C^{-}$$

whenever, the cathode potential of thyristor T_1 becomes more with respect to mode potential, thyristor T_1 gets turned off.

During the off state of the thyristor 'T $_{\rm i}$ ', due to the presence of stored energy in the inductor, current flows through the load whose path may be given as

Diode 'D' is known as blocking diode. The associated waveforms are as shown in fig. 4.23(b).

4.17 AC CHOPPERS

The desired ac voltage magnitudes may be obtained by two methods:

- By using stepup and stepdown transformers, in which the change in voltage depends upon the transformation ratio (k) of the transformer.
- 2. By using Ac choppers
- Ac choppers are those voltage changing or voltage varying circuits which

4.66 Power E

Circuit description description description is shown in fig. 4.24(a)

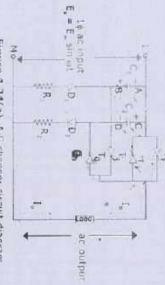


Figure 4.24(a) A.C chopper circuit diagram

It consists of two main thyristors T_1 , T_2 and two auxiliary thyristors T_3 and T_4 , C_1 and C_2 are the commutating capacitors where as diodes D_1 and D_2 provides the charging path for these capacitors. Thyristors T_1 and T_3 may be used for producing the positive alternation and thyristors T_2 and T_4 for negative alternation of input ac voltage.

Principle of operation may be explained in different modes

Mode 0: In this mode, during positive half cycle of ac supply voltage, capacitor C_2 gets charged whose path may be given as

$$L = C_1 = D_2 = R_2 = N$$

During negative half cycle, the capacitor C1 gets charged through the path.

$$M - R_1 - D_1 - C_1 - L$$

with the polarities as shown in circuit diagram.

For commutation of the main SCRs T_1 and T_2 , the voltage across these capacitors may be used.

Mode 1: During the positive half cycle of the supply voltage, thyristor T_1 is torward based which may be triggered at the instant T_1 with a firing angle α . The current flows through the path as shown.

$$L = T_1 - load - M_1$$

At the instant t_2 , the auxiliary thyristor T_3 may be turned on so that the capacitor C_1 gets discharged through it. It's path may be given as

$$C_B - T_3 - T_1 - C_A$$

Whenever the discharging current becomes more than the forward current of T_1 , thyristor T_1 gets commutated. The auxiliary thyristor T_3 may be turned off naturally at the instant t_3 as the current passes through natural zero.

Hence, SCRs T_1 and T_3 forms the first pair for producing the positive alternation of the input ac voltage

Mode 2 operation: During negative half cycle of the supply voltage, thyristor T_2 is forward biased which may be triggered at the instant t_4 . The load current follows the path

when the instantaneous voltage reaches the instant t_8 , auxiliary thyristor T_4 may be triggered. As soon as the auxiliary thyristor gets turned on the capacitor C_2 gets discharged whose discharging current path may be given as

$$C_C - T_2 - T_4 - C_{rec}$$

When this discharging current becomes more than the load current, SCR Γ_1 becomes turned off. At the instant r_6 , SCR T_4 gets automatically turned off due to natural zero. Again at instant r_7 , SCR T_1 gets triggered and the above process repeats. Its associated waveform is as shown in Fig.4.24(b).

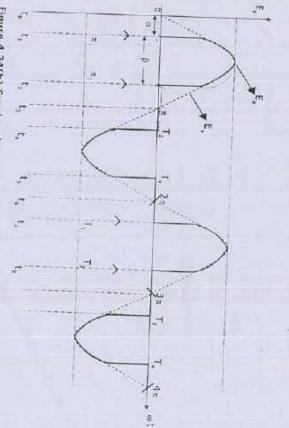
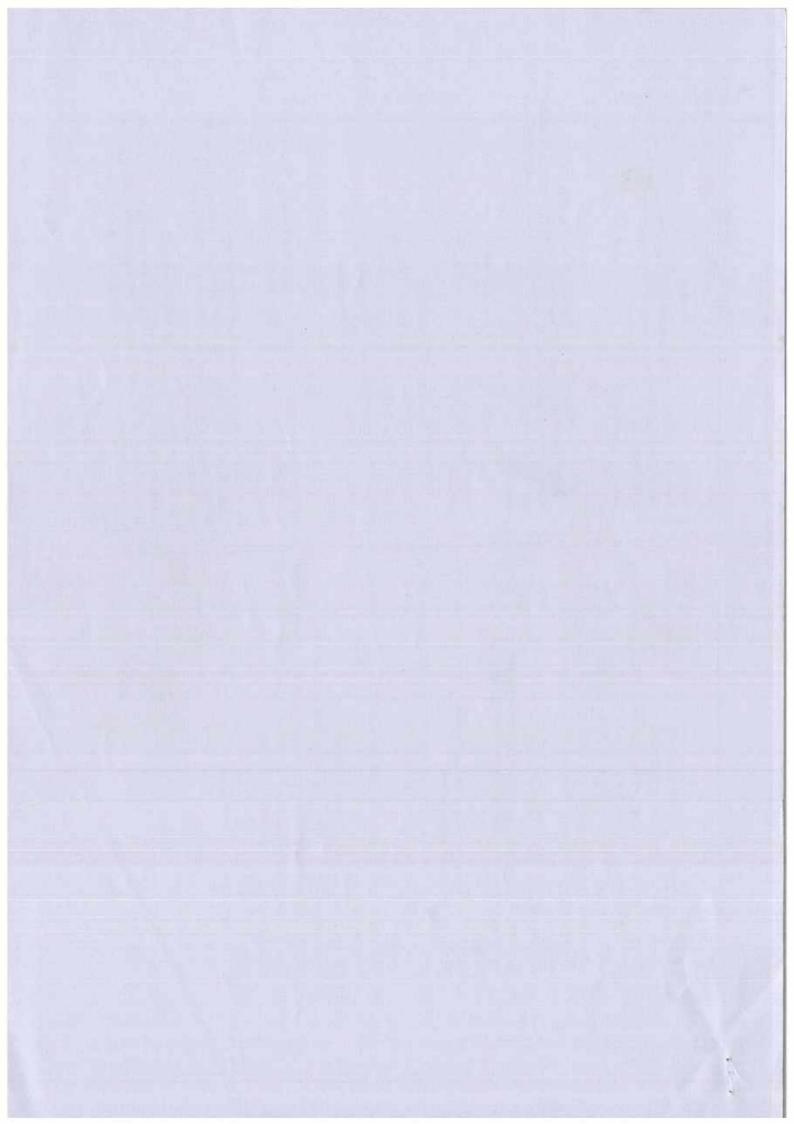
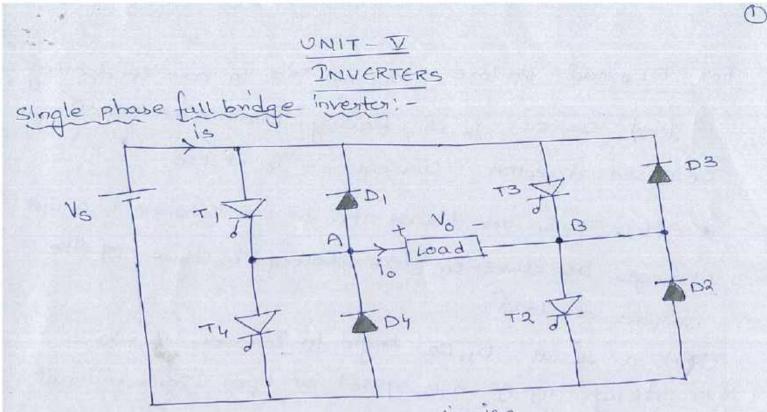


Figure 4.24(b) Supply voltage and output voltage waveforms in an A.C. Chopper

Chrispers 4.69	Problems 1. The input voltage of a step down chopper being 220v, the load voltage is 100v. Assuming a chopping frequency of 5kHz, find the ON and OFF intervals of the thyristors in each cycle.	Ans: $I_{on} = 90.9 \mu_{Sec}$ $T_{orr} = 109.1 \mu_{Sec}$	 A stepup chopper has a supply voltage of 100v while output voltage is 250v. If the off period of chopper is 150µsec determine the parton of the 			or	 the average output voltage and current ii. output current at the tustant of commutation iii. freewheeling diods and commutation 	iv. rms values of output voltage and cms currents.	Ans: (i) 15v, 0.1875A (ii) 0.625A (iii) 0 (iv) 27.38V, 0.342A. (v) 0.1875A 0.247A	f00	Error ton - 20H Sec.	 A stype A chopper, if the constant supply voltage is 300v and the load being 500, find the average, rms values of the output voltage and chopper time. Assume duty cycle α = 0.6 Ans: E_{o(avg)} = 179.4 V. E_{orms} = 231.60v; η = 99.66% A chopping circuit is operating on TRC principle at a frequency of 4kHz on a 440v dc supply. If the load voltage is 200v, Compute the conduction and mon conduction period of thyristor in each cycle, and the duty cycle. T_{ON} = 0.113 m sec. T_{OFF} = 0.137 m sec.
	 EXERCISE Explain the optimating principle of both stepup and stepdown choppers involving different moder with the neat circuit diagrams. Derive an expression for output voltage in terms of duty cycle for a stepup, stepdown and step down/on chonner. 		 What type of commutation process does D/C chopper undergoes? Explain different type of commutation processes involved in chopper with suitable waveforms. 	Describe different types of chopper circuit.	 Explain the working of first quadrant or type A chopper with suitable voltage and current waveforms. Give the complete time domain analysis of type A chopper. 	 Obtain the expressions for l_{omax} and l_{omin} for type A chopper and also derive expression for per unit ripple current. 	 Describe the continuous and discontinuous modes of operation involved in type A chopper and get the average load current expression for this type of chopper. 	 With a neat sketch, explain the working principle of type B and type C choppers. 	 Give the detailed analysis of type D chopper. Explain the working principle of type E chopper with a neat sketch. 	 With the circuit diagram and waveforms, explain the working of Jones chopper. Give the design consideration of D.C Jones chopper and mention the advantages of it over other chopper circuits. 	14. Write short notes on	er b. AC chopper

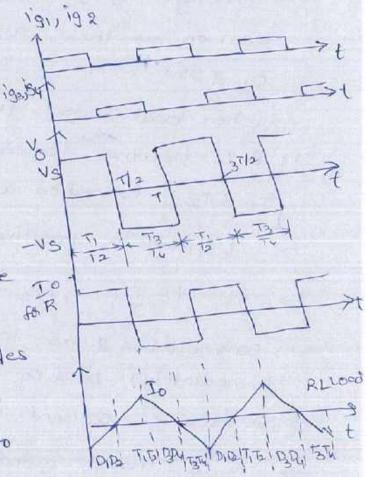
4.68 Pawe





-> For bad Restative load, four sces would suffice because load awarent to \$ No would always be in phase with each other.

> For other than the originative loads, awarent is will not be inphase with rollage Vo et diades connected in antiparallel with scres will allow the awarent to flow when the main tryristors



are turned off. -> As the energy is fed back to the descure when there diades conduct, there are called feedback diads (PI) D2,D3(D4) For RLoload: Before to, sars T38 Ty are conducting & load current to is flowing from BtoA ie; in reversed direction: Current = - To at to. > After T3; Ty are twined off at to; current is cannot change its direction immediately because of the nature of load.

-> As a stepult D1, D2 begin to conduct, Vo = Vs. > Though T1, T3 are gated at (=0, sere will not twom on as these are oreverse biased by V.D across D1 & P2'

> when boud Convent through D1/D2 fails to 3 ero)
TI & T2 become torroard biased by source holtage Vs.
TI & T2. through on as these are gated for a period 7/55.
> is flows in positive direction for a to B.
> At t= T; T1, T2 are hund off by forced commutation & as load correct Cannot reverse immediately) D3 & Al come into conduction to allow
> Di flow of correct is after 7/2.

-> T3, Ty though gated, will not two on as these are oneverse blaced by the roltage abop in diodes D3, D4

-> when awarent in diades D3, Dy drops to Beno, T3, Ty are twired on as there are abready galed

UNIT – I POWER SEMI CONDUCTOR DEVICES

Objective:

To study the different types of power semiconductor devises and their switching characteristics

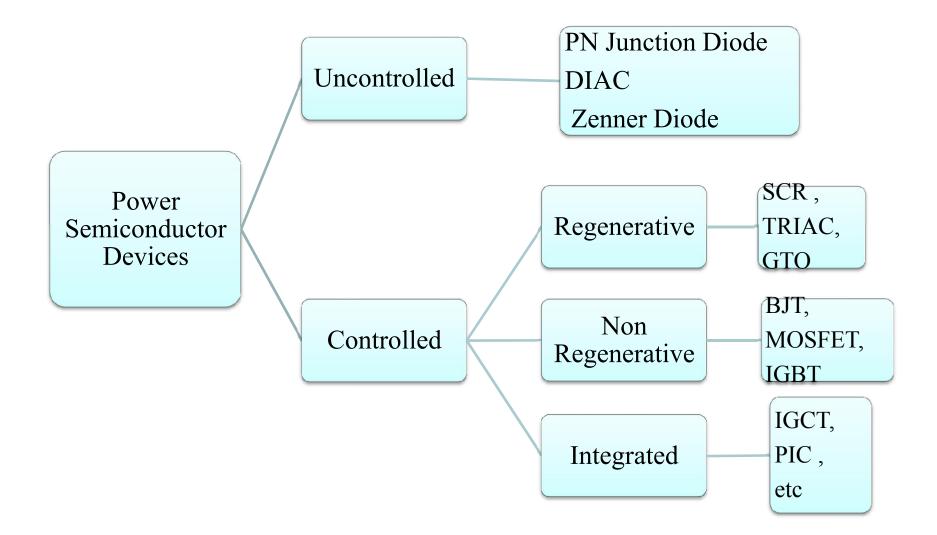
Topics to be covered:

- Introduction on power semiconductor devises
- Power diode static and dynamic characteristics
- Seasic theory of operation thyristor (SCR)
- SCR Static (steady state) characteristics
- ✤ TRIAC, GTO characteristics
- Dynamic characteristics of SCR
- Power BJT steady state and switching characteristics
- ✤ Power MOSFET steady state and switching characteristics
- Power IGBT steady state and switching characteristics

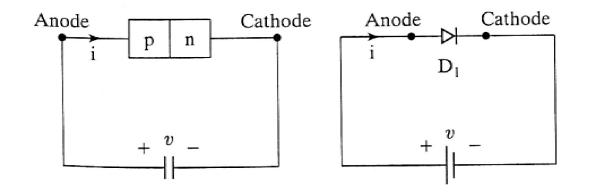
POWER DEVICES

- Voltage, current and power ratings are much higher than the conventional devises.
- Switching speed is also much higher than the conventional devices.

CLASSIFICATION



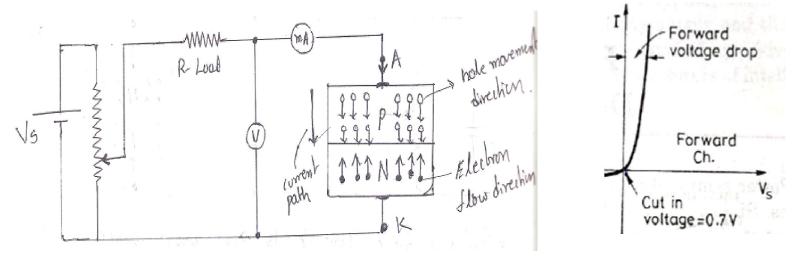
PN-JUNCTION DIODE



Forward Bias :- Diode Anode terminal is connected to more positive than the cathode terminal.

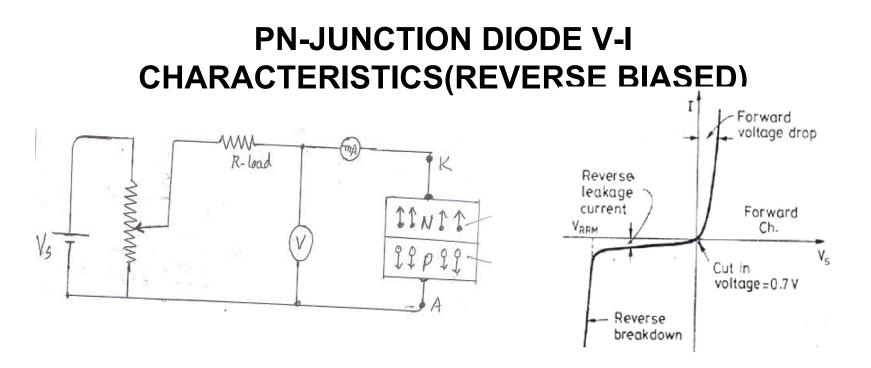
Reverse Bias :- Diode cathode terminal is connected to more positive than the anode terminal.

PN-JUNCTION DIODE V-I CHARACTERISTICS(FORWARD BIASED)



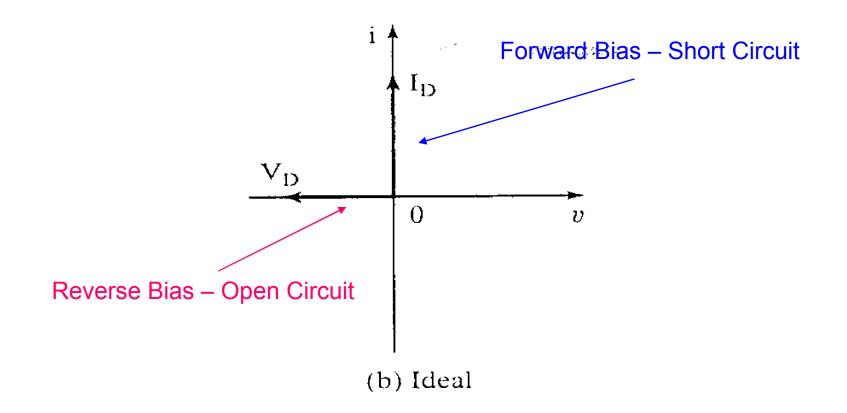
➤When source voltage greater than cut in or threshold or turn on voltage diode current rises rapidly .

- ≻Diode offers less impedance in forward bias
- ≻Diode act as closed switch during forward bias.
- ≻Forward voltage drop across diode is typically 0.8v to 1v

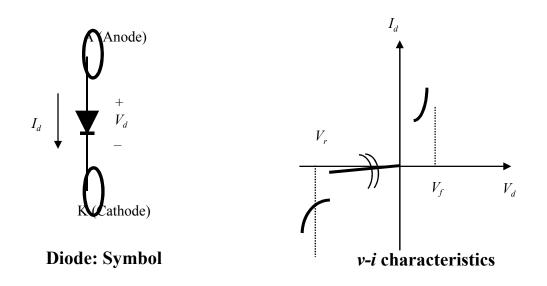


- By increasing reverse voltage across diode small amount of leakage current will flow from cathode to anode terminal.
- By keep on increasing reverse voltage at particular instant diode junction will break down and starts conduction and diode get damage.
- > Diode offers high impedance in reverse bias (V<V_{RRM})
- Diode act as open switch during reverse bias
- Diodes are available up to 3000A and 5KV

IDEAL DIODE V-I CHARACTERISTIC

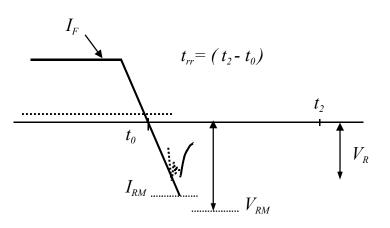


Power Diode



- When diode is forward biased, it conducts current with a small forward voltage (V_f) across it (0.2-3V)
- When reversed (or blocking state), a negligibly small leakage current (uA to mA) flows until the reverse breakdown occurs.
- Diode should not be operated at reverse voltage greater than V_r

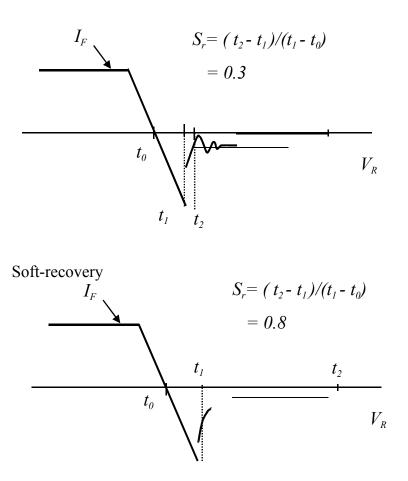
Reverse Recovery



- When a diode is switched quickly from forward to reverse bias, it continues to conduct due to the *minority carriers* which remains in the p-n junction.
- The minority carriers require finite time, i.e, t_{rr} (reverse recovery time) to recombine with opposite charge and neutralise.
- Effects of reverse recovery are increase in switching losses, increase in voltage rating, over-voltage (spikes) in inductive loads

Softness factor, S_r

Snap-off



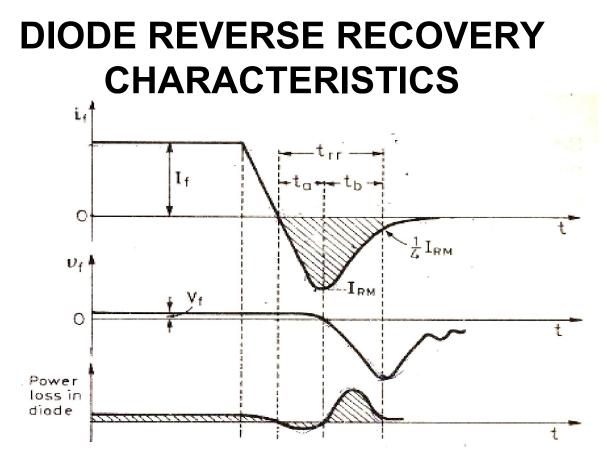
Power Electronics and Drives (Version 3-2003). Dr. Zainal Salam, UTM-JB

Types of Power Diodes

- Line frequency (general purpose):
 - On state voltage: very low (below 1V)
 - Large t_{rr} (about 25us) (very slow response)
 - Very high current ratings (up to 5kA)
 - Very high voltage ratings(5kV)
 - Used in line-frequency (50/60Hz) applications such as rectifiers
- Fast recovery
 - Very low t_{rr} (<1us).
 - Power levels at several hundred volts and several hundred amps
 - Normally used in high frequency circuits
- Schottky
 - Very low forward voltage drop (typical 0.3V)
 - Limited blocking voltage (50-100V)
 - Used in low voltage, high current application such as switched mode power supplies.

DIODE REVERSE RECOVERY CHARACTERISTICS

- After the forward diode current decays to zero, the diode continues to conduct in the reverse direction
- The reverse current flows for a time called reverse recovery time t_{rr}



>t_{rr} is the time required for the diode to regain its blocking capability.

- >t_a is the time to remove the stored charge from the depletion region of the junction
- >t_b is the time to remove the stored charge from two P N layers

TYPES OF POWER DIODES

➢Based on reverse recovery time power diodes are classified as

$$t_{rr} = t_a + t_b$$

Softness or S factor = t_{b/t_a}

>S factor =1 Soft Recovery diode

S factor <1 fast Recovery diode

Soft Recovery or General-purpose or line frequency diode:

✓ trr is 25µsec

 \checkmark Available rating up to 5kV and 4KA

✓Used in rectifiers, ups, battery chargers, welding and electrical traction.

Fast Recovery Diode:-

 \checkmark trr is less than 5µsec

✓ Available rating up to 3kV and 3KA

Schotty Diode:-

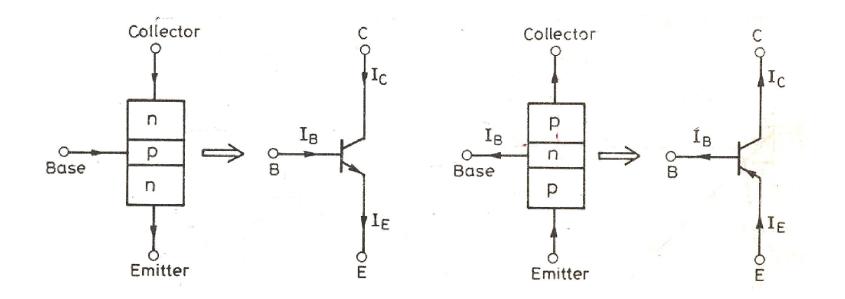
✓ trr is less than 50nsec

 \checkmark Available rating up to 400V

✓ Used in SMPS, High Frequency Instrumentation,

DC-DC converters etc

BJT



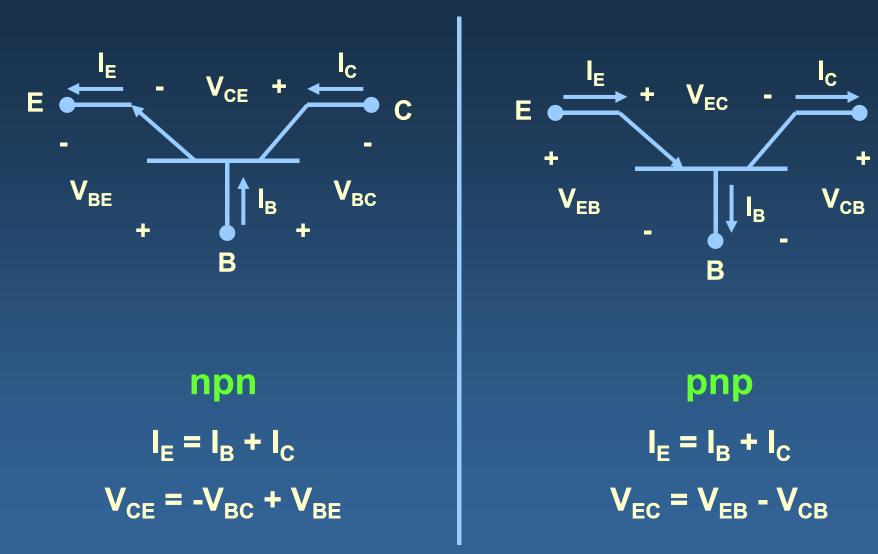
POWER BJT

- Three layer ,Two Junction npn or pnp type
- **Bipolar** means current flow in the device is due to the movement of BOTH holes and Electrons.

The BJT – Bipolar Junction Transistor The Two Types of BJT Transistors: npn pnp p Ε Ε С С n n n р р **Cross Section Cross Section** B B B В **Schematic Schematic Symbol** Symbol Ε

- Collector doping is usually ~ 10⁶
- Base doping is slightly higher ~ 10⁷ 10⁸
- Emitter doping is much higher ~ 10¹⁵

BJT Relationships - Equations

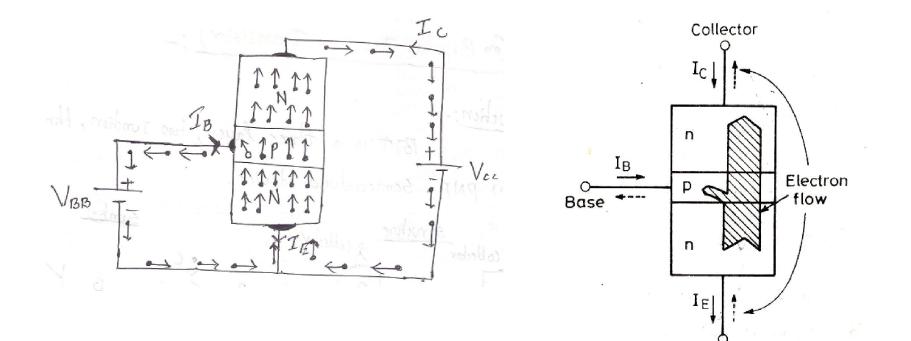


Note: The equations seen above are for the transistor, not the circuit.

Kristin Ackerson, Virginia Tech EE Spring 2002

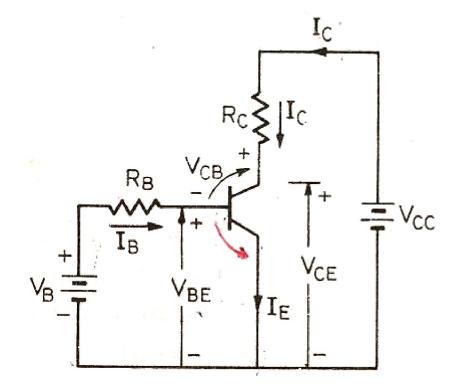
С

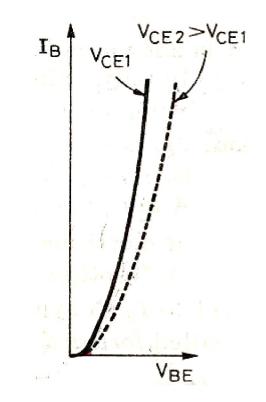
WORKING OPERATION OF BJT



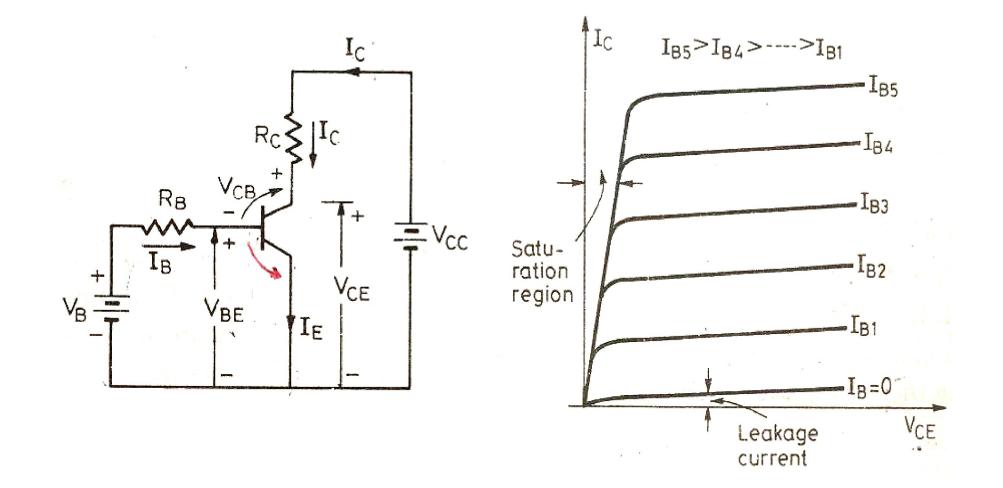
Emitter

INPUT CHARACTERISTICS

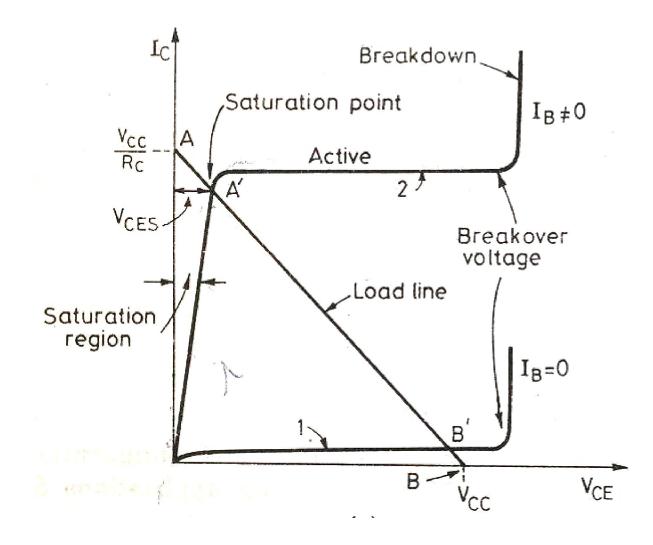




OUTPUT CHRACTRESTICS



TRANSISTOR ACT AS SWITCH



$$I_{CS} = \frac{V_{CC} - V_{CES}}{R_C}$$
$$I_{BS} = \frac{I_{CS}}{\beta}$$

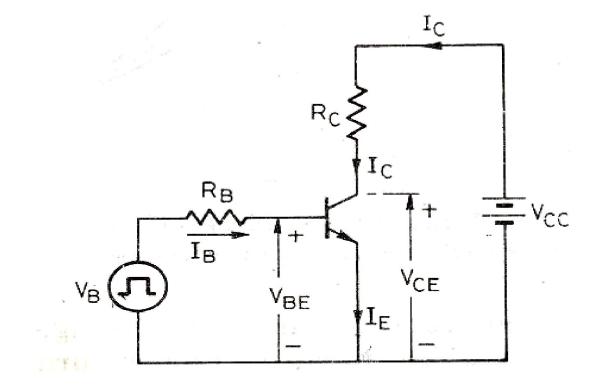
> If base current is less than I_{BS} the transistor operates in the active region or some where between saturation and cut off region .

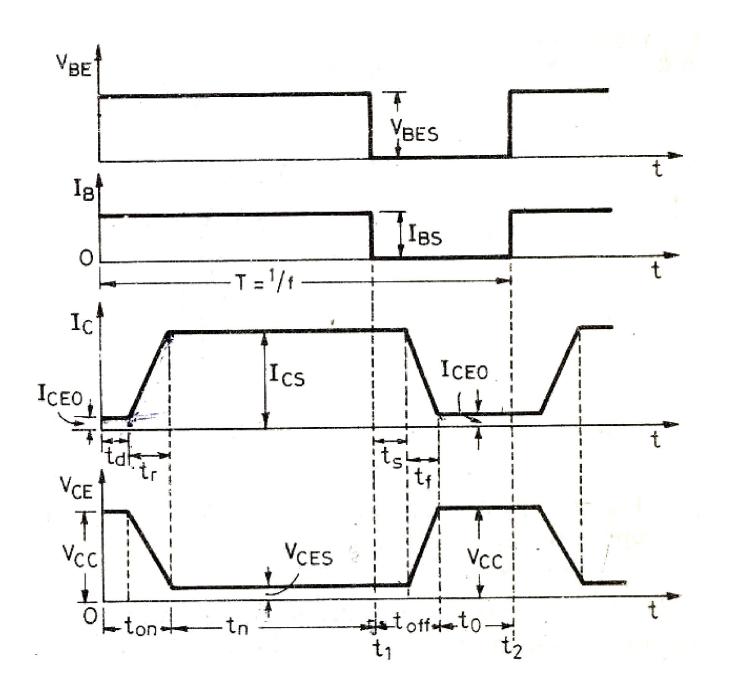
> If base current is greater than I_{BS} hard drive of the transistor is obtained .

≻Over drive factor

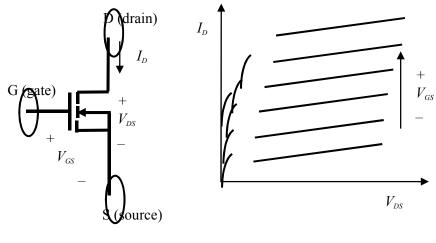
$$ODF = \frac{I_B}{I_{BS}}$$

SWITCHING CHARACTERISTICS

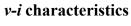




Metal Oxide Silicon Field Effect Transistor (MOSFET)





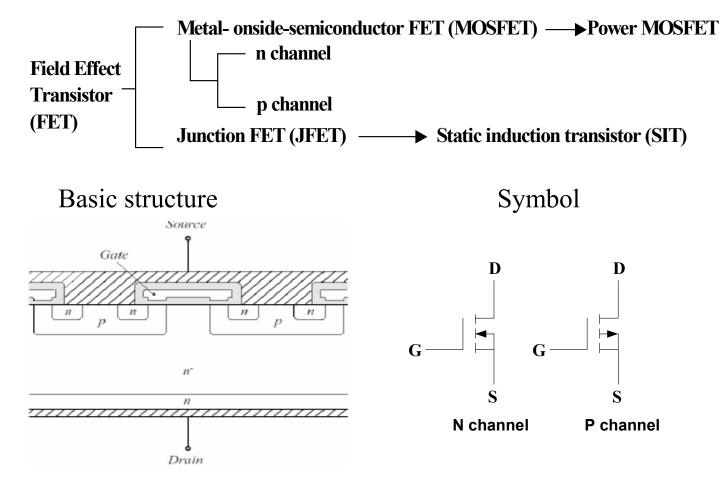


- **Ratings:** Voltage $V_{DS} < 500$ V, current $I_{DS} < 300$ A. Frequency f > 100KHz. For some low power devices (few hundred watts) may go up to MHz range.
- Turning on and off is very simple.
 - To turn on: $V_{GS} = +15V$
 - To turn off: $V_{GS} = 0$ V and 0V to turn off.
- Gate drive circuit is simple

1.4.3 Power metal- oxide- semiconductor field effect transistor—

Power MOSFET

A classification



POWER MOSFET

- Three Terminals Drain, source And Gate
- Voltage Controlled Device
- Power MOSFET has much higher current handling capability in ampere range and drain to source blocking voltage(50-100V) than other MOSFETs
- Gate Circuit Impedance Is High (Of The Order Of Mega Ohm).Hence Gate Can Be Driven Directly From Microelectronic Circuits.
- Used In Low Power High Frequency

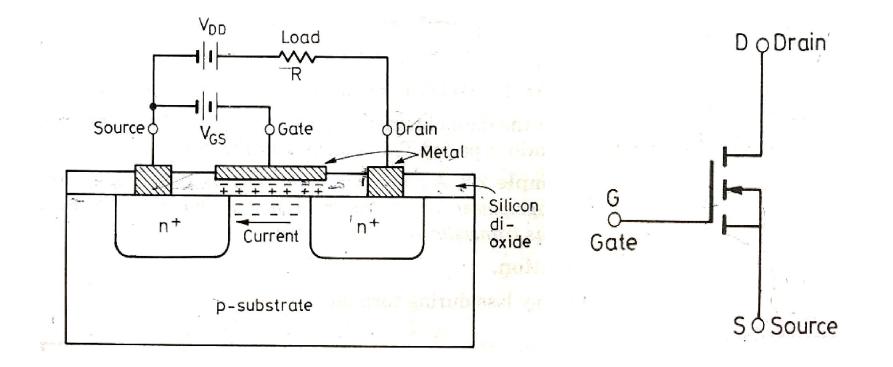
MOSFET characteristics

- Basically low voltage device. High voltage device are available up to 600V but with limited current. Can be paralleled quite easily for higher current capability.
- Internal (dynamic) resistance between drain and source during on state, $R_{DS(ON)}$, limits the power handling capability of MOSFET. High losses especially for high voltage device due to $R_{DS(ON)}$.
- Dominant in high frequency application (>100kHz). Biggest application is in switchedmode power supplies.
 - **Ratings:** Voltage V_{DS} <500V, current I_{DS} <300A. Frequency f>100KHz. For some low power devices (few hundred watts) may go up to MHz range.
 - Turning on and off is very simple.
 - To turn on: $V_{GS} = +15$ V
 - To turn off: $V_{GS} = 0$ V and 0V to turn off.
 - Gate drive circuit is simple

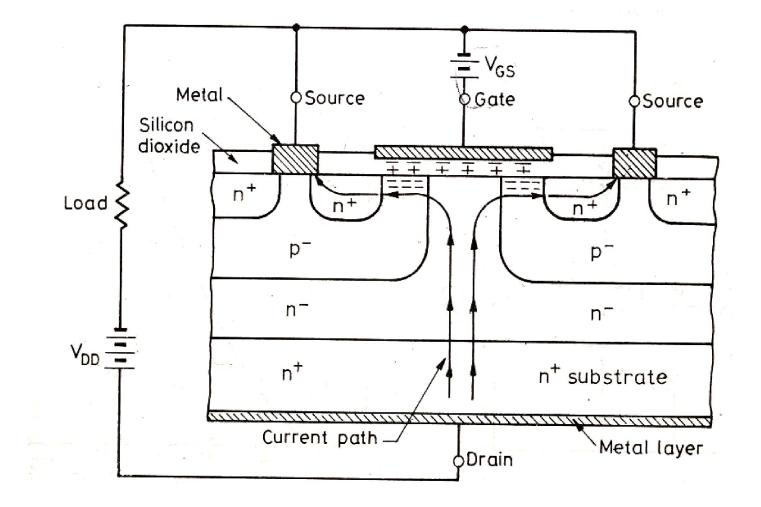
MOSFET Terminals

- The voltage applied to the GATE terminal determines whether current can flow between the SOURCE & DRAIN terminals.
- For an n-channel MOSFET, the SOURCE is biased at a lower potential (often 0 V) than the DRAIN
 (Electrons flow from SOURCE to DRAIN when VG > VT)
- For a p-channel MOSFET, the SOURCE is biased at a higher potential (often the supply voltage VDD) than the DRAIN (Holes flow from SOURCE to DRAIN when VG < VT)

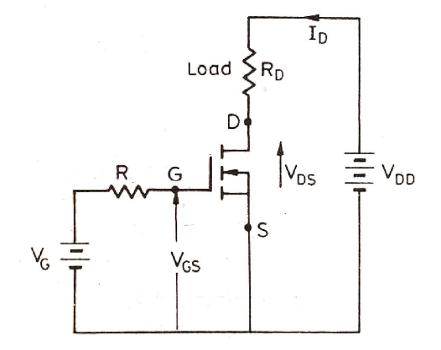
MOSFET(LOW POWER)

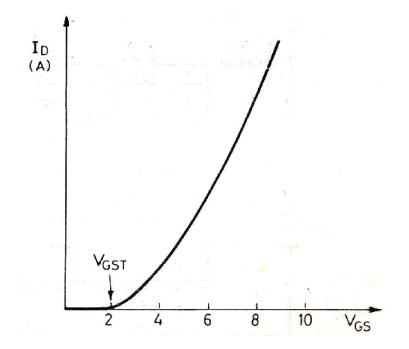


MOSFET(High Power)

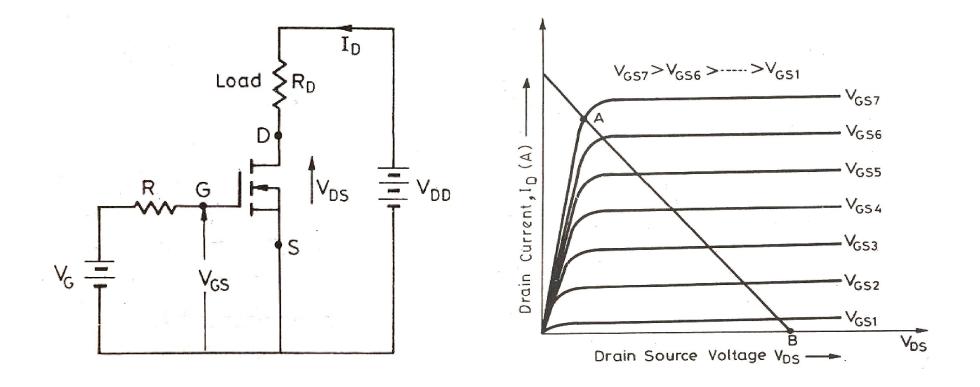


TRANSFER CHARACTERISTICS

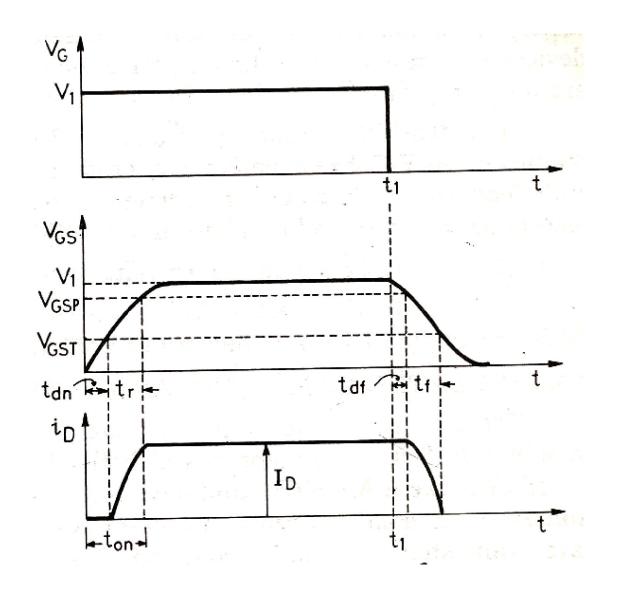




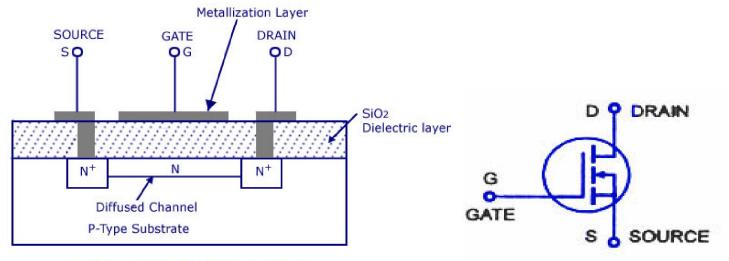
OUTPUT CHARACTERISTICS



SWITCHING CHARACTERISTICS

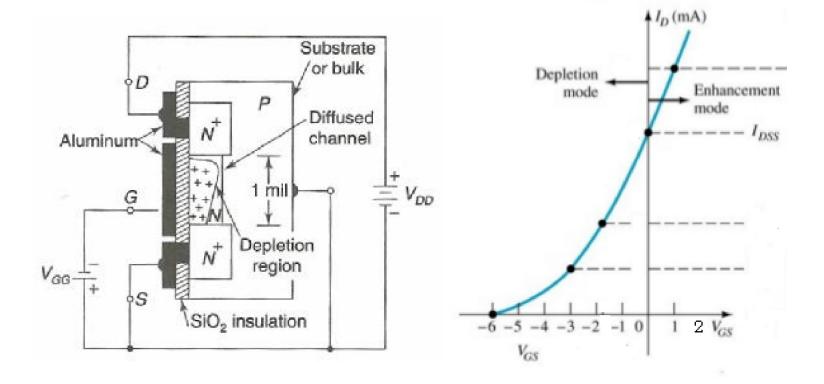


DE MOSFET

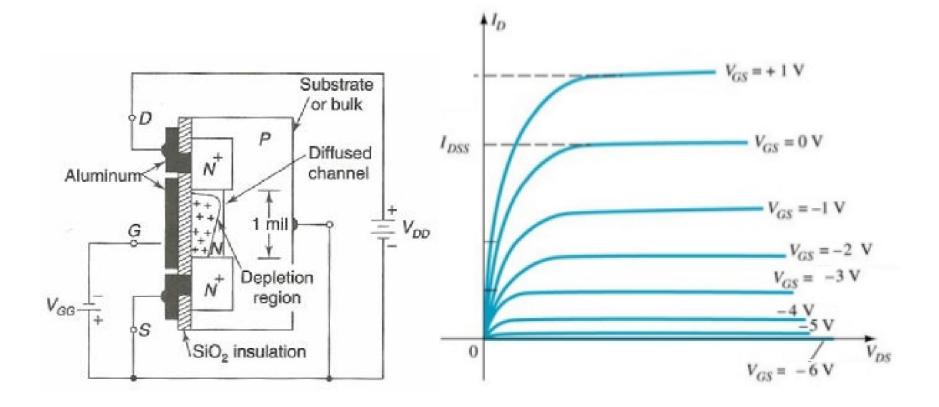


N-Channel DE-MOSFET Structure

TRANSFER CHARACTERISTICS



OUTPUT CHARACTERISTICS



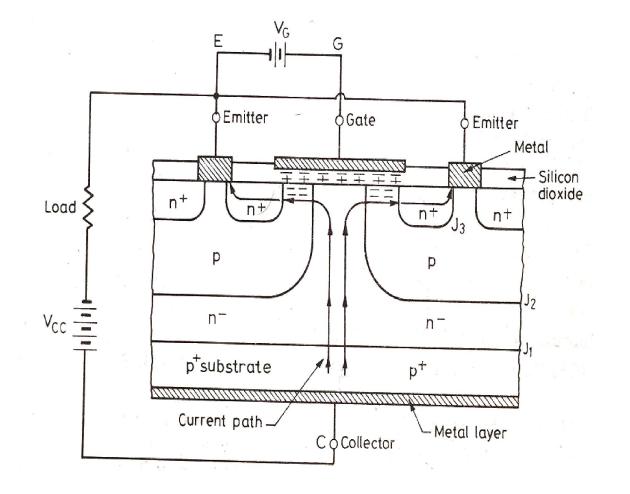
COMPARISON OF BJT AND MOSFET

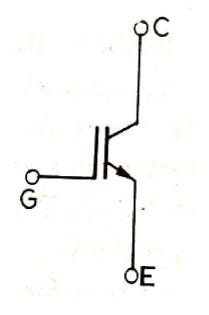
S.No	BJT	MOSFET
1	Bipolar Device	Unipolar Device
2	Low input impedance(kilo ohm)	High input impedance (mega ohm)
3	High switching losses but lower conduction losses	Lower switching losses but high on- resistance and conduction losses
4	Current controlled device	Voltage controlled device
5	Negative temperature coefficient of resistance. parallel operation is difficult. current sharing resistors should be used.	Positive temperature coefficient of resistance. parallel operation is easy
6	Secondary breakdown occurs.	Secondary breakdown does not occur.
7	Available with ratings 1200v,800a	Available with ratings 500v,140a

INSULATED GATE BIPOLAR TRANSISTOR (IGBT)

- COMBINES THE BEST QUALITIES OF BOTH **BJT** AND
 MOSFET
- HAS HIGH INPUT IMPEDANCE AS MOSFET AND HAS
 LOW ON-STATE POWER LOSS AS IN BJT
- OTHER NAMES
 - ✓ **MOSIGT** (METAL OXIDE INSULATED GATE TRANSISTOR),
 - ✓ **COMFET** (CONDUCTIVELY-MODULATED FIELD EFFECT TRANSISTOR),
 - ✓ **GEMFET** (GAIN MODULATED FIELD EFFECT TRANSISTOR),
 - ✓ **IGT** (INSULATED GATE TRANSISTOR)

IGBT BASIC STRUCTURE

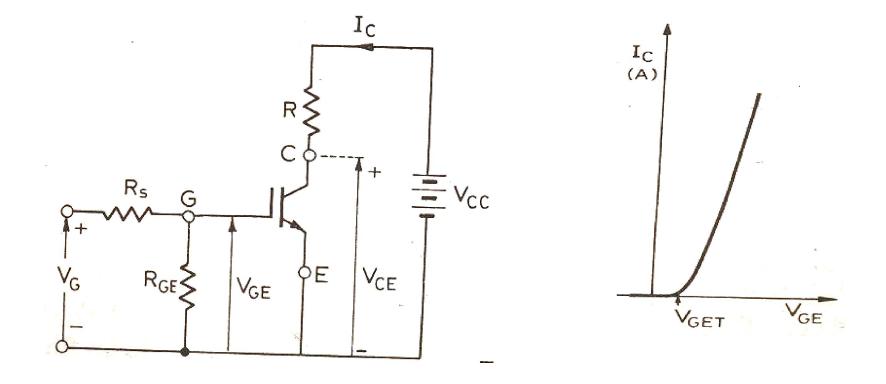




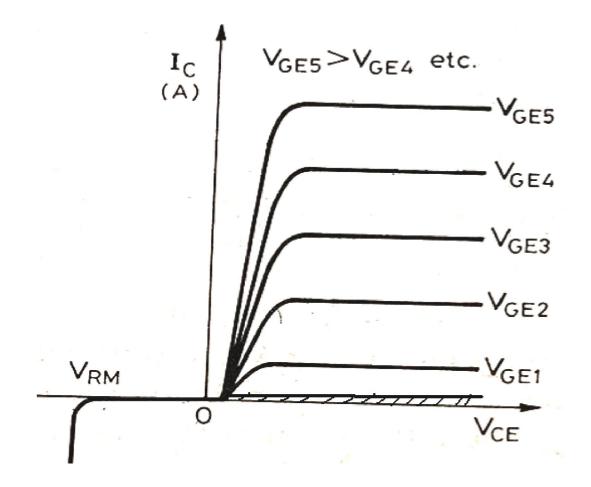
Insulated Gate Bipolar Transistor (IGBT)

- Combination of BJT and MOSFET characteristics.
 - -Gate behaviour similar to MOSFET easy to turn on and off.
 - -Low losses like BJT due to low on-state Collector-Emitter voltage (2-3V).
- **Ratings:** Voltage: V_{CE}<3.3kV, Current,: I_C<1.2kA currently available. Latest: HVIGBT 4.5kV/1.2kA.
- Switching frequency up to 100KHz. Typical applications: 20-50KHz.

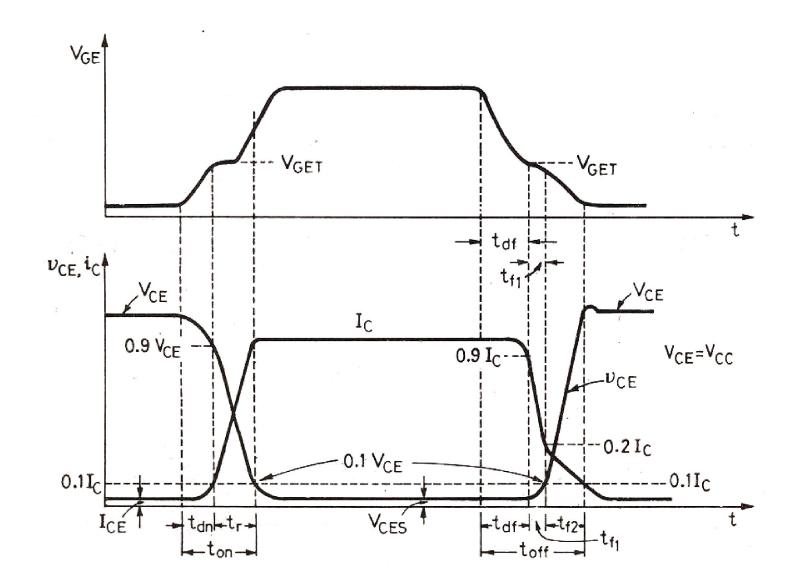
TRANSFER CHARACTERISTICS



OUTPUT CHARACTERISTICS



DYNAMIC CHARACTERISTICS



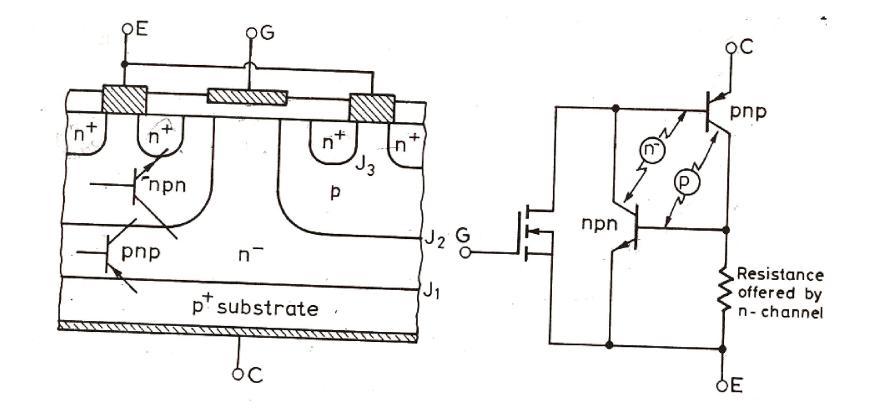
COMPARISON OF IGBT WITH MOSFET

S.No	MOSFET	IGBT
1.	Three terminals are Gate, source and drain.	Three terminals are Gate, emitter and collector
2.	High input impedance	High input impedance
3.	Voltage controlled device	Voltage controlled device
4.	Ratings available up to 500V,140A	Ratings available up to 1200V,500A
5.	Operating frequency is up to 10Mhz	Operating frequency is up to 10khz
6.	With rise in Temperature, the increase in on-state resistance in MOSFET is mor pronounced than IGBT. SO, on-state voltage drop and losses rise rapidly i MOSFET than in IGBT rise in temperature.	
7.	with rise in voltage, the increment in on-state voltage drop is more dominant i MOSFET than it is in IGBT. this means IGBTS can be designed for higher voltage ratings than MOSFETS.	

APPLICATIONS OF IGBT

- DC AND AC MOTOR DRIVES
- UPS SYSTEMS, POWER SUPPLIES
- DRIVES FOR SOLENOIDS, RELAYS AND CONTACTORS

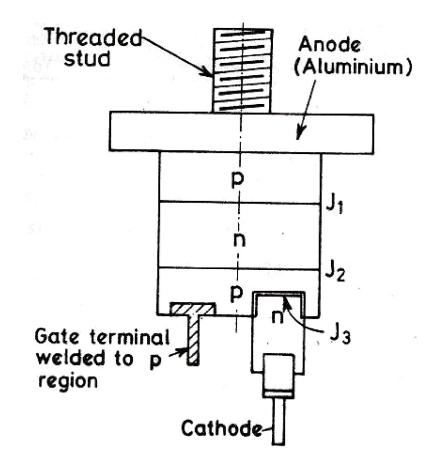
IGBT EQUIVALENT CIRCUIT



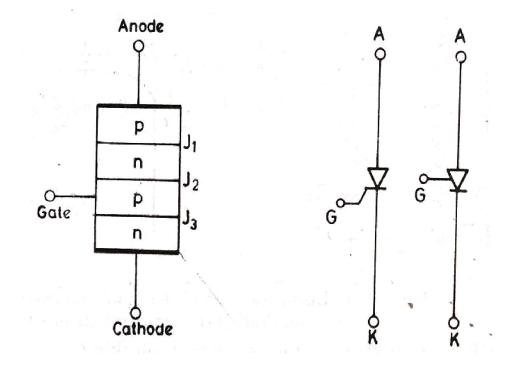
THYRISTOR FAMILY DEVISES

- SCR (Silicon Controlled Rectifier)
- TRIAC(Bidirectional thyristor)
- DIAC (Bidirectional thyristor)
- SUS (Silicon Unilateral Switch)
- SCS (Silicon Controlled Switch)
- LAT (Light Activated Thyristor)
- GTO (Gate turn off Thyristor)
- RCT (Reverse Conduction Thyristor)
- SITHS (Static Induction Thyristor)

THYRISTOR



THYRISTOR STRUCTURE AND SYMBOL

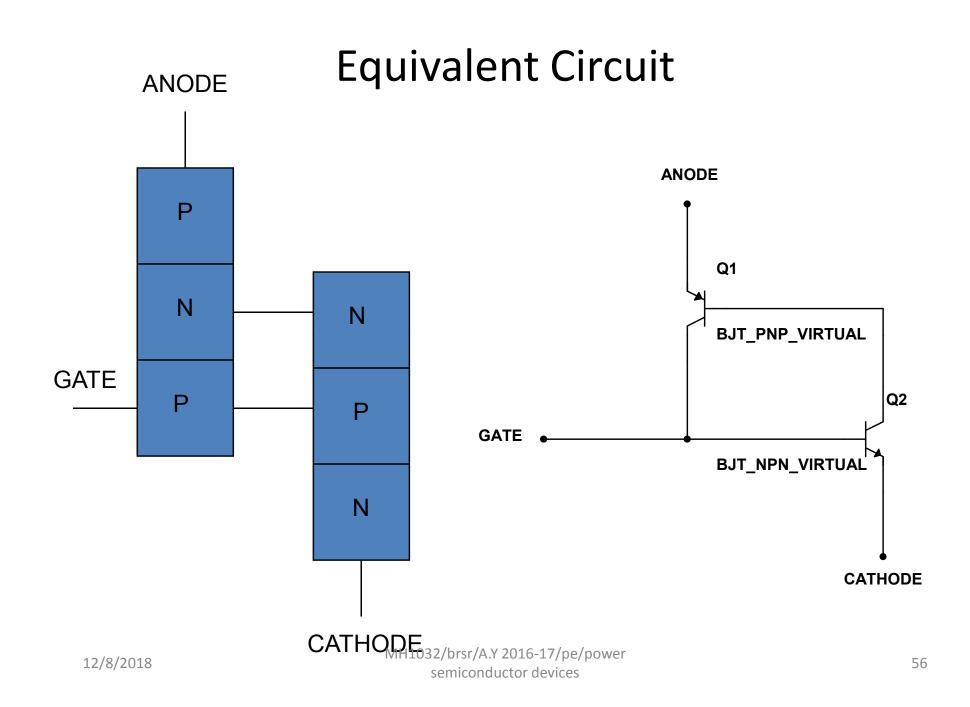


SILICON CONTROLLED RECTIFIER (SCR)

- Three terminal, four layers (P-N-P-N)
- Can handle high currents and high voltages, with better switching speed and improved breakdown voltage .
- Name 'Thyristor', is derived by a combination of the capital letters from **THYRatron** and **transISTOR**.
- Has characteristics similar to a thyratron tube But from the construction view point belongs to transistor (pnp or npn device) family.

SCR/ Thyristor

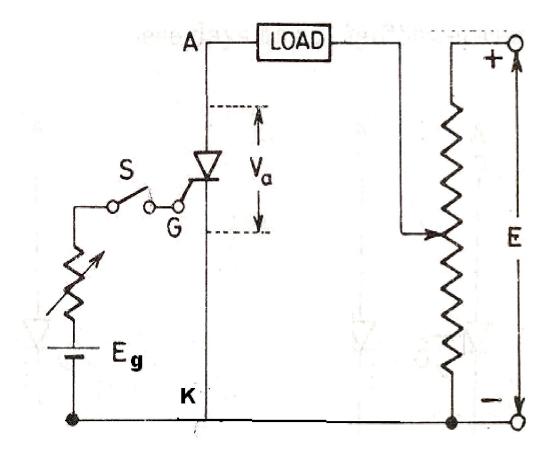
- An SCR (Thyristor) is a "controlled" rectifier (diode)
- SCR is an unidirectional device
- Thyristor also blocks the current flow from anode to cathode until it is triggered into conduction by proper gate signal between gate and cathode terminals



SCR OPERATING REGIONS

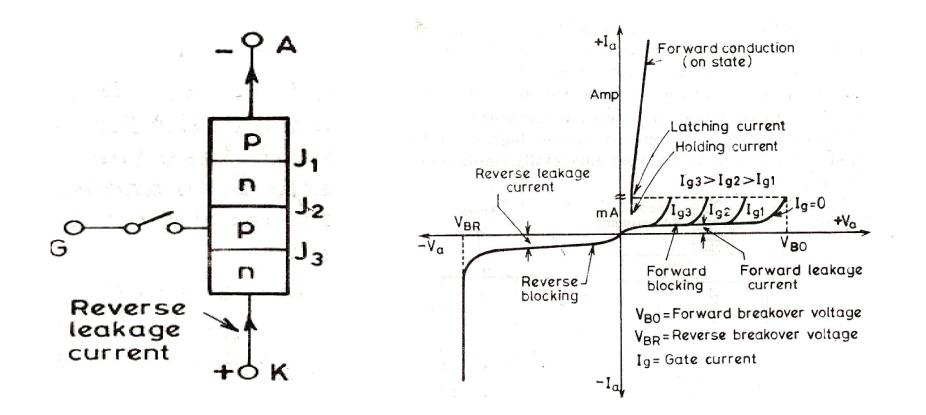
- Reverse blocking mode
- Forward blocking mode
- Forward conduction mode

STATIC V-I CHARACTERISTICS

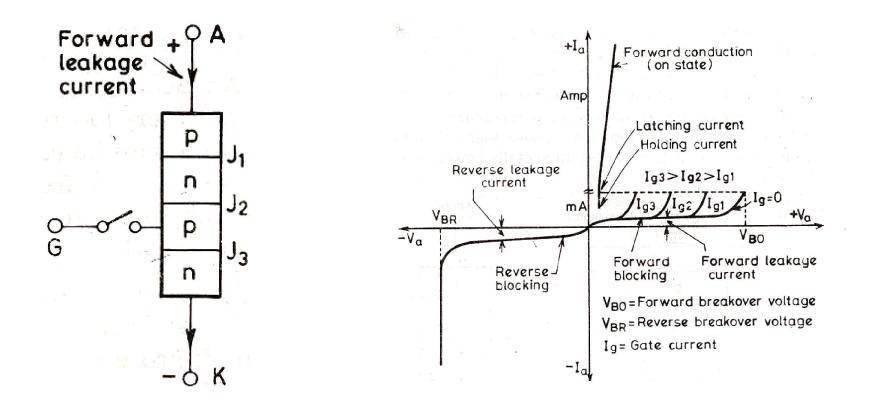


- Thyristors can only be turned on with three conditions:
- 1. The device must be forward biased, i.e., the anode should be more positive than the cathode.
- 2. A positive gate current (Ig) should be applied at the gate.
- 3. The current through the thyristor should be more than the latching current. Once conducting ,the anode current is LATCHED (continuously flowing).

REVERSE BLOCKING MODE



FORWARD BLOCKING MODE



- Latching Current: This is the minimum anode current required to turn on the SCR device and convert it from the Forward Blocking State to the ON State.
- Holding Current: This is the minimum forward current flowing through the thyristor in the absence of the gate triggering pulse.
- Forward Breakover Voltage: This is the forward voltage required to be applied across the thyristor to turn it ON without the gate signal application.
- Max Reverse Voltage: This is the maximum reverse voltage to be applied across the thyristor before the reverse avalanche occurs.

SCR OPERATING MODES

FORWARD BLOCKING MODE: Anode is positive w.r.t cathode, but the anode voltage is less than the break over voltage (VBO).

only leakage current flows, so thyristor is not conducting .

- **FORWARD CONDUCTING MODE:** When anode voltage becomes greater than VBO, thyristor switches from forward blocking to forward conduction state, a large forward current flows.
 - If the IG=IG1, thyristor can be turned ON even when anode voltage is less than VBO.
 - The current must be more than the latching current (IL).
 - If the current reduced less than the holding current (IH), thyristor switches back to forward blocking state.
- **REVERSE BLOCKING MODE:** When cathode is more positive than anode, small reverse leakage current flows. However if cathode voltage is increased to reverse breakdown voltage, Avalanche breakdown occurs and large current flows.

Thyristor-Operation Principle

- Thyristor has three p-n junctions (J1, J2, J3 from the anode).
- When anode is at a positive potential (VAK) w.r.t cathode with no voltage applied at the gate, junctions J1 & J3 are forward biased, while junction J2 is reverse biased.
 - As J2 is reverse biased, no conduction takes place, so thyristor is in forward blocking state (OFF state).
 - Now if *V*AK (forward voltage) is increased w.r.t cathode, forward leakage current will flow through the device.
 - When this forward voltage reaches a value of breakdown voltage (VBO) of the thyristor, forward leakage current will reach saturation and reverse biased junction (J2) will have avalanche breakdown and thyristor starts conducting (ON state), known as forward conducting state.
- If Cathode is made more positive w.r.t anode, Junction J1 & J3 will be reverse biased and junction J2 will be forward biased.
- A small reverse leakage current flows, this state is known as reverse blocking state.
- As cathode is made more and more positive, stage is reached when both junctions A & C will be breakdown, this voltage is referd as reverse breakdown voltage (OFF state), and device is in reverse blocking state

64

Anode

J

J2

J3

Cathode

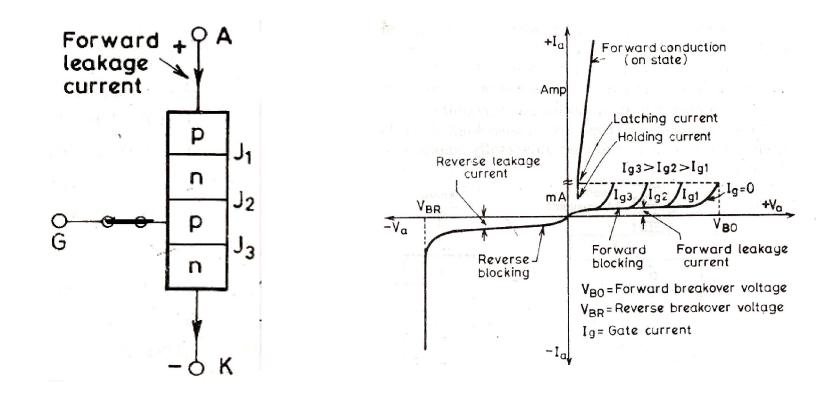
P

Ν

P

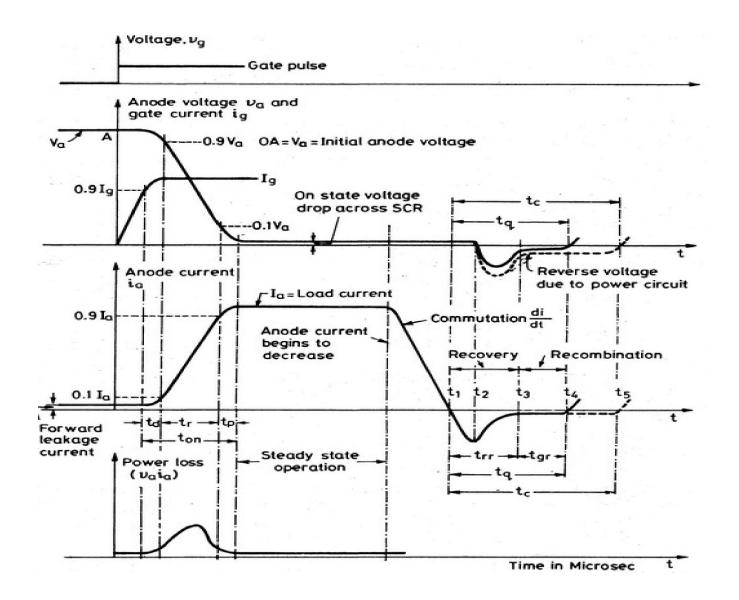
N

FORWARD CONDUCTION MODE



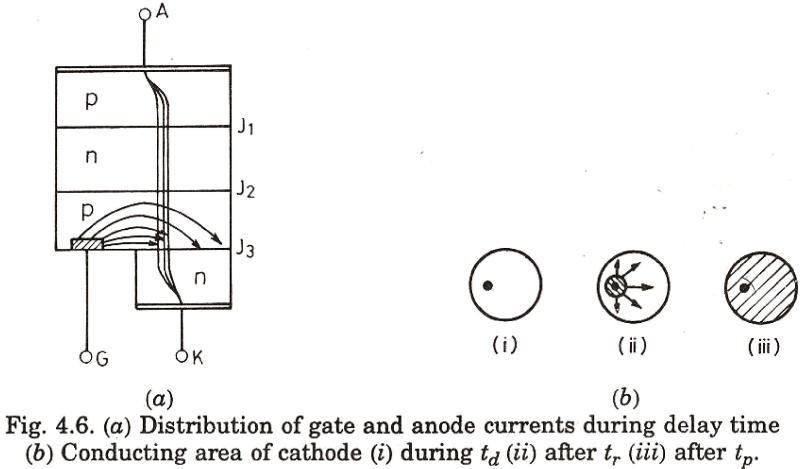
Once SCR is turned on it looses gate control.

SWITCHING CHARACTERISTICS OF SCR

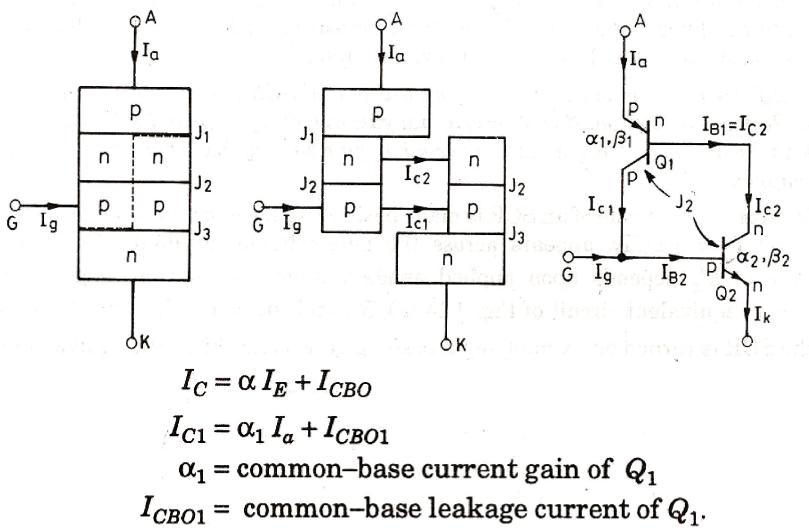


Turn on time (t_{on}) :- $(t_d + t_r + t_P)$ > Delay time (t_d) > Rise time (t_r) > Spread time (t_P)

Turn off time(t_{off}):- (t_{rr} +t_{gr}) ≻Reverse recovery time(t_{rr}) ≻Reverse recovery time(t_{gr})

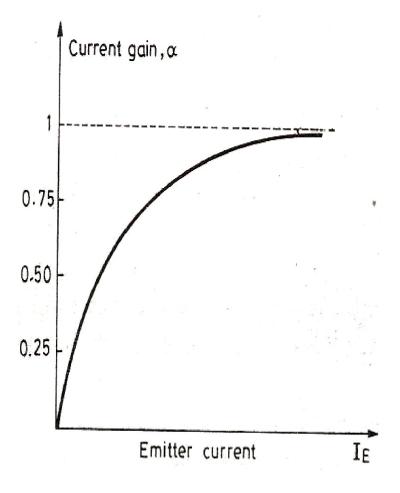


TWO TRANSISTOR MODEL OF SCR



$$\begin{split} I_{C2} &= \alpha_2 \, I_k + I_{CBO2} \\ \alpha_2 &= \text{common-base current gain of } Q_2 \\ I_{CBO2} &= \text{common-base leakage current of } Q_2 \\ I_k &= \text{emitter current of } Q_2. \end{split}$$

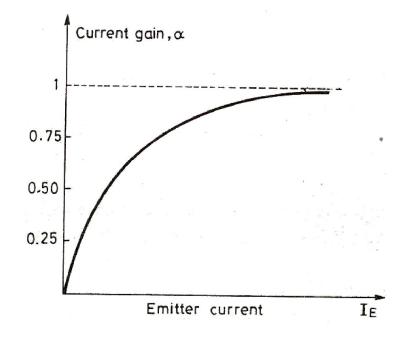
$$I_{a} = I_{C1} + I_{C2} I_{a} = \alpha_{1} I_{a} + I_{CBO1} + \alpha_{2} I_{k} + I_{CBO2} I_{a} = \alpha_{1} I_{a} + I_{CBO1} + \alpha_{2} (I_{a} + I_{g}) + I_{CBO2} I_{a} = \frac{\alpha_{2} I_{g} + I_{CBO1} + I_{CBO2}}{1 - (\alpha_{1} + \alpha_{2})}$$

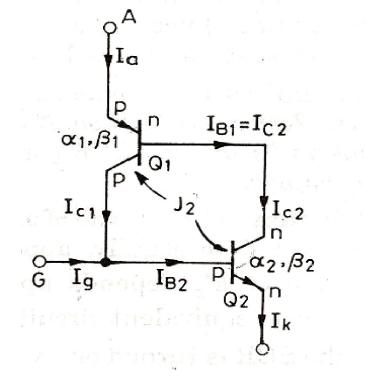


TURN ON METHODS OF SCR

- Gate triggering
- Forward voltage triggering
- dv/dt triggering
- Temperature triggering
- Light triggering

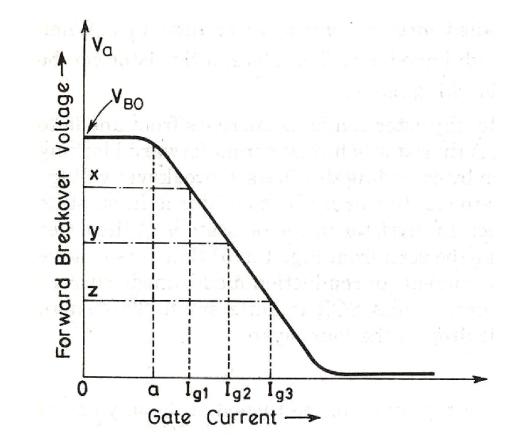
GATE TRIGGERING METHOD





$$I_{a} = \frac{\alpha_{2} I_{g} + I_{CBO1} + I_{CBO2}}{1 - (\alpha_{1} + \alpha_{2})}$$

GATE TRIGGERING



FORWARD VOLTAGE TRIGGERING

- In forward voltage triggering voltage is applied between anode and cathode with gate circuit open, junction j₂ is reverse biased.
- The width of depletion layer across junction j₂ decreases with an increase in anode cathode voltage
- If forward voltage across anode-cathode is gradually increases ,the depletion layer across junction j₂ will decrease.
- When voltage reaches to forward break over voltage depletion region completely vanished and device will turns on

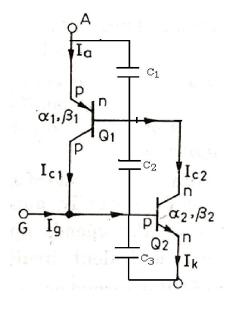
dV/dT TRIGGERING METHOD

♦ With forward voltage across anode & cathode of a thyristor, two outer junctions (A & C) are forward biased but the inner junction (J2) is reverse biased.

The reversed biased junction J2 behaves like a capacitor because of the space-charge present there.

✤If a voltage ramp is applied across the anode-to-cathode, a current will flow in the device to charge the device capacitance according to the relation:

$$i = C_j \frac{dv_a}{dt}$$



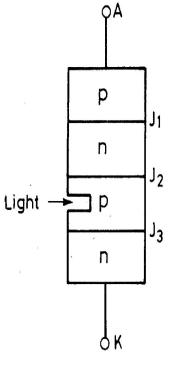
This method of triggering is not desirable because high charging current (Ic) may damage the thyristor.

TEMPERATURE TRIGGERING

- During forward blocking, most of the applied voltage appears across reverse biased junction J2.
- This voltage across junction J2 associated with leakage current may raise the temperature of this junction.
- With increase in temperature, leakage current through junction J2 further increases.
- This cumulative process may turn on the SCR at some high temperature.
- High temperature triggering may cause Thermal runaway and is generally avoided.

Light triggering

- In this method light particles (photons) are made to strike the reverse biased junction, which causes an increase in the number of electror hole pairs and triggering of the thyristor.
- For light-triggered SCRs, a slot (niche) is made ir the inner p-layer.
- When it is irradiated, free charge carriers are generated just like when gate signal is applied b/w gate and cathode.
- Pulse light of appropriate wavelength is guided by optical fibers for irradiation.
- If the intensity of this light thrown on the recess exceeds a certain value, forward-biased SCR is turned on. Such a thyristor is known as lightactivated SCR (LASCR).
- Light-triggered thyristors is mostly used in highvoltage direct current (HVDC) transmission systems.



SCR TURN OFF METHODS

Natural commutation

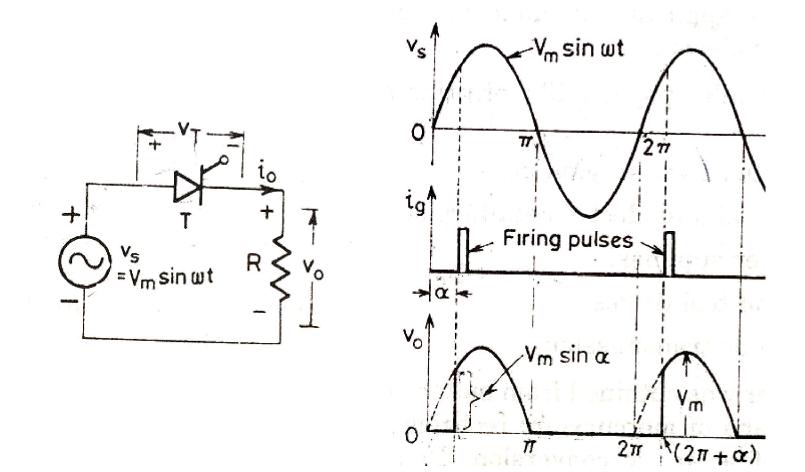
Forced commutation

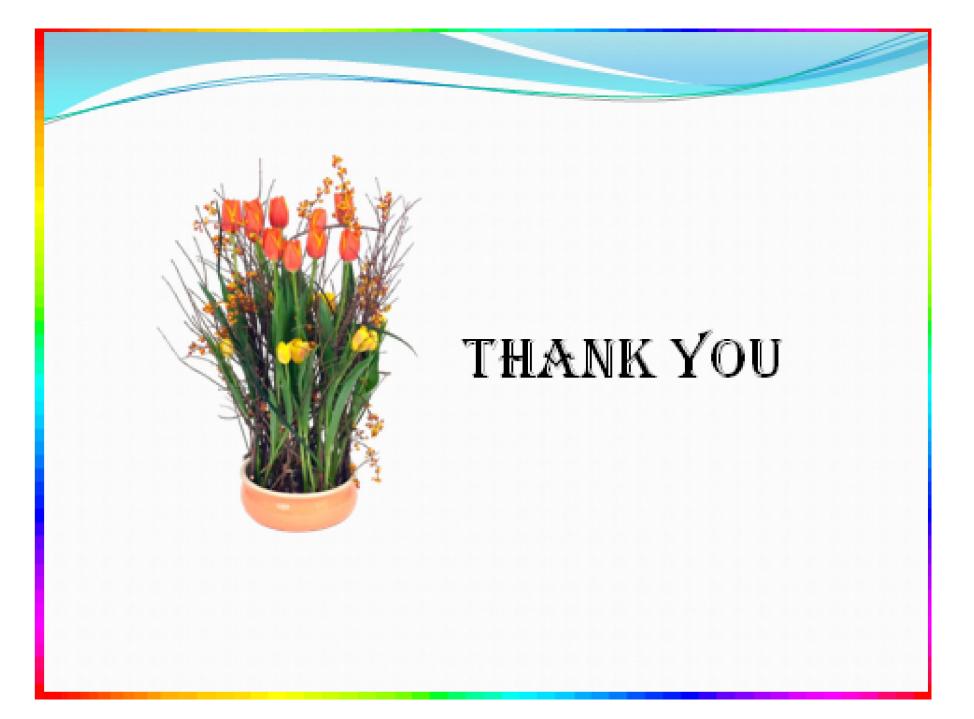
- The process of turning OFF SCR is defined as "Commutation".
- Thyristor cannot be turned off by applying negative gate current. It can only be turned off if the current *I* through it goes negative (reverse).
- In all commutation techniques, a reverse voltage is applied across the thyristor during the turn OFF process.
- There are two methods by which a thyristor can be turned OFF.
- i. Natural Commutation ii. Forced Commutation

- Natural Commutation
- In AC circuit, the current always passes through zero for every half cycle.
- As the current passes through natural zero, a reverse voltage will simultaneously appear across the device. This will turn OFF the device immediately.
- This happens when negative portion of the of sine-wave occurs. This process is called as "natural commutation" since no external circuit is required for this purpose.

- Forced Commutation
- Another method of turning off is known as "forced commutation".
- The anode current is "diverted" to another circuitry.
- To turn OFF a thyristor, the forward anode current should be brought to zero for sufficient time to allow the removal of charged carriers.
- In case of DC circuits the forward current should be forced to zero by means of some external circuits.

LINE COMMUTAATION





GR14

SET-1

III-year B.Tech I semester Regular Examinations, May/June -2016 Power Electronics

(EEE)

Time: 3 hours

PART - A

Answer all the questions, all questions carry equal marks

10*2 Marks = 20 Marks

Max Marks: 70

1. a. Define Latching current and Holding current of a Thyristor.	[2]
b. Give the details of Snubber circuit.	[2]
c. Distinguish between Midpoint type and Bridge type connections used in converter topology.	[2]
d. A 230V,50Hz supply is given to a 1-phase Half wave controlled converter which is delivering power load R= 10 Ω , for a firing angle delay of 60 [°] , Calculate the average value of output Voltage.	wer to [2]
e. List out the advantages of Three phase converters over single phase converters.	[2]
f. Write down the type of commutation technique used in Inverter in which if the Switching device i) SCR ii) MOSFET	is [2]
i) SCR ii) MOSFET	[2]
i) SCR ii) MOSFETg. Write the principle of operation of Cyclo-converter and classify them?	[2] [2]

$\mathbf{PART} - \mathbf{B}$

Answer any FIVE questions. All questions carry equal marks

5*10 Marks = 50 Marks

2. a) Explain Dynamic V - I characteristics of an SCR and mention the salient points.	[5]
b) Describe the types of commutation of an SCR, explain in detail.	[5]
3. a) Analyse 1-Phase Half wave controlled converter for $\alpha = 45^{\circ}$ with RLE-Load and derive the exp for RMS value of output.	pression [5]
b) Explain about Line commutated Inverters and derive the expression for RMS value of output v	voltage. [5]
4. a) Describe about Three phase six pulse converters with the help of wave forms.b) Explain the operation of Basic series Inverter with the help of waveforms.	[5] [5]
5. a) Explain the operation of AC voltage controller designed using TRIAC and write down the a value of the converter?	average [5]
	c ·

b) Obtain the waveforms of a Cyclo-converter in which the output voltage frequency is 1/3 rd of input frequency, if input Frequency Fs = 50 Hz. [5]

6. a) Describe different control strategies of a Chopper.	[5]
b) Analyse the principle of operation of Morgan's chopper with the help of waveforms.	[5]
7. a) Explain the modes of operation of an SCR.	[5]
b) Define Active power Input and Reactive power Input to the converters. And	[5]
Give the purpose of freewheeling diode in three phase semi converter circuit with RL-load.	[5]
8. a) A 1-Phase AC regulator feeds power to a resistive load of 4Ω from 230v ac supply. C V_{rms} , for a firing angle of 60° .	alculate V ₀ , [5]
b) Describe the operation of Boost converter with the help of waveforms.	[5]

MODEL QUESTION PAPER-2

III-year B.Tech I semester Regular Examinations, May/June -2016

Power Electronics

(Electrical and Electronics Engineering)

Time: 3 hours

Max Marks:70

PART-A

Answer ALL questions. All questions carry equal marks

10*2 Marks=20 Marks

1(a) What is Holding Current?	[2]
(b) Define String Efficiency.	[2]
(c) Determine the average and RMS output voltages of single phase full converter.	[2]
(d) Define overlap angle.	[2]
(e) Express the advantages of freewheeling diode.	[2]
(f) What is the principle of operation of Inverters?	[2]
(g) Derive the expression for the Power dissipated in the load, for a single phase	
AC voltage controller feeding Resistive load.	[2]
(h) Determine the applications of Cycloconverter.	[2]
(i) What are the different control strategies of Choppers?	[2]
(j) What is Duty Ratio?	[2]

PART-B

Answer any FIVE questions. All questions carry equal marks.

5*10 Marks = 50 Marks

2(a) Explain the working of Class-D commutation circuit with neat circuit diagram and	
waveforms.	[5]
(b) Draw the equivalent circuit of a UJT and explain its working.	[5]
3(a) Describe the operation of a single phase two pulse midpoint converter with	[5]
relevant waveforms. Derive an expression for average output voltage.	
(b) Explain the effect of source inductance in full converter with relevant waveforms.	[5]
4 (a) Explain the operation of three phase, half wave controlled converter with R	[5]
load for $\alpha = 60^0$ with relevant waveforms.	
(b)What are the different pulse width modulation techniques used for inverters. [5]	
5 (a) Derive the expressions for the Power dissipated in the load, for a single	[5]
phase AC voltage controller feeding Resistive-inductive load for discontinuous op	peration of current.
(b) Explain the operation of the single phase bridge type cycloconverter with RL load	
for Continuous conduction.	[5]
6 (a) Explain the operation of DC Morgan's Chopper for resistive load with neat circuit	
diagram and output voltage and current waveforms.	[5]
(b) Explain the operation of a basic dc chopper and obtain the average output voltage	
and current as a function of Edc, R and duty cycle δ .	[5]
7 (a) Explain the parallel operation of SCR's	[5]
(b) Draw and explain the simple SCR series inverter circuit employing class A type	[5]
commutation with the help waveforms.	
8 (a) A step-up chopper with a pulse width of 150 μ s operating on 220V, dc supply.	[5]
Compute the load voltage if the blocking period of the device is 40 μ s.	
(b) A single phase full wave ac voltage controller has a resistance load of 10ohms.	[5]
The input ac voltage is 230V, 50Hz. For a delay angle of 90° , determine the rms load current, rms thyristor current and input powerfactor for above two loads.	ad voltage, rms





Department of Electrical & Electronics Engineering Assignment Questions and Solutions

Unit-1

- 1. Explain the series and parallel operation of SCR's.
- 2. Explain the construction and static V-I characteristics of SCR clearly with neat diagrams.
- 3. Define triggering. What are the different turn-on methods of SCR? Explain.
- 4. List out and explain the Voltage and Current ratings of SCR.
- 5. Explain the two transistor analogy of SCR with necessary conclusions.
- 6. Explain the necessity of Snubber circuit for SCR and give its operation.
- 7. Define the commutation. Describe the types of forced commutation of an SCR, explain in detail.
- 8. Explain different types of firing circuits of SCR.

Unit-2

- 1. Describe the operation of a single phase **semi converter** RLE Load by using freewheeling diode with relevant waveforms. Derive an expression for average output voltage.
- 2. Explain the operation of single phase **half wave converter** with RL-Loadat $\alpha = 60^{\circ}$ with necessary wave forms. Also derive the output voltage, output current and RMS output voltages
- 3. Explain the operation of single phase **full wave bridge converter** for RLE load at a $\alpha = 60^{\circ}$ with necessary output wave waveforms. Also derive the output voltage, output current & RMS voltage equation.
- 4. a) Give the difference between midpoint and bridge type convertersb) Give the difference between discontinuous mode and continuous mode of operation
- 5. a) Differentiate between fully controlled and half controlled Converters.b) Explain about Line commutated Inverters and derive the expression for RMS value of output voltage.
- 6. A single phase half wave converter is operated from a 120v,60Hz supply. If the load is resistive of value 10 ohms and delay angle is alpha is 60⁰. Determine i) the efficiency ii)formfactor iii)ripple factor iv) Transformer utilization factor v)peak inverse voltage of thyristor



Department of Electrical & Electronics Engineering

7. Explain the effect of source inductance in full converter with relevant waveforms with R L Load.

Unit-3

- 1) Explain the operation of 3 phase half wave controlled rectifier (3-pulse Converter) with resistive load and also derive the average and RMS load voltage.
- 2) Explain the operation of 3 phase full wave controlled rectifier (6-pulse Converter) with resistive load and also derive the average and RMS load voltage.
- 3) Explain the operation of single phase full bridge voltage source inverter and the help of voltage and current waveforms?
- 4) Explain the operation of single phase half bridge voltage source inverter.
- 5) Explain the operation of parallel inverter with neat circuit and waveforms.
- 6) Explain the operation of Basic series Inverter with the help of waveforms.
- 7) Describe different types of pulse width modulation techniques (PWM) inverter.
- 8) Explain about Voltage Control Techniques for Inverter.



Department of Electrical & Electronics Engineering

Previous University Question Papers

- 1(a) What is Holding Current?
- (b) Define String Efficiency.
- (c) Determine the average and RMS output voltages of single phase full conveter
- (d) Define overlap angle.
- (e) Express the advantages of freewheeling diode.
- (f) What is the principle of operation of Inverters?
- (g) Derive the expression for the Power dissipated in the load, for a single phase AC voltage controller feeding Resistive load.
- (h) Determine the applications of Cycloconverter
- (i) What are the different control strategies of Choppers?
- (j) What is Duty Ratio?

2(a) Explain the working of Class-D commutation circuit with neat circuit diagram and waveforms.

(b) Draw the equivalent circuit of a UJT and explain its working. [5+5]

3(a) Describe the operation of a single phase two pulse midpoint converter with relevant waveforms. Derive an expression for average output voltage.

(b) Explain the effect of source inductance in full converter with relevant waveforms. [5+5]

4 (a) Explain the operation of three phase, half wave controlled converter with R load for $\alpha = 600$ with relevant waveforms.

(b)What are the different pulse width modulation techniques used for inverters.

5 (a) Derive the expressions for the Power dissipated in the load, for a single phase AC voltage controller feeding Resistive-inductive load for discontinuous operation of current.

(b) Explain the operation of the single phase bridge type cycloconverter with RL load for Continuous conduction

6 (a) Explain the operation of DC Morgan's Chopper for resistive load with neat circuit diagram and output voltage and current waveforms.

(b) Explain the operation of a basic dc chopper and obtain the average output voltage

and current as a function of Edc, R and duty cycle δ .

7 (a) Explain the parallel operation of SCR's

(b) Draw and explain the simple SCR series inverter circuit employing class A type commutation with the help waveforms.



Department of Electrical & Electronics Engineering

8 (a) A step-up chopper with a pulse width of 150 μs operating on 220V, dc supply.

Compute the load voltage if the blocking period of the device is 40 µs.

(b) A single phase full wave ac voltage controller has a resistance load of 10ohms. The input ac voltage is 230V, 50Hz. For a delay angle of 900, determine the rms load voltage, rms load current, rms thyristor current and input powerfactor for above two loads.



Department of Electrical & Electronics Engineering

Academic Year	COURSE OBJECT : 2018-2019	VES	
Semester	: I		
Name of the Program:	EEE B.Tech	III/I	Section: B
Course/Subject: Power E	lectronicCode:C	GR15A3018	
Name of the Faculty: D.K Designation: Assistant p		Dept:	EEE

On completion of this Subject/Course the student shall be able to:

S.No	Course Objectives
1.	Introduction to different switching devices and their characteristics
2.	Analysis of converters and voltage control techniques
3.	Visualization of different waveforms for converters.
4.	Understanding and deriving mathematical model for practical systems.
5.	Skill of applying Power electronic techniques to different machines and observing their characteristics

Signature of HOD faculty

Signature of

Date:

Date:



Department of Electrical & Electronics Engineering

Academic Year	COURSE OU : 2018-2019			
Semester	: I			
Name of the P	Program: EEE	B.Tech .	III/I	Section: B
Course/Subject: P	Power Electronic	Code:	GR15A3018	
Name of the Facult	ty: D.Karunakumar	D	Dept:	EEE
Designation: Assi	istant professor			

The expected outcomes of the Course/Subject are:

S.No	Course Outcomes
1.	Discuss the basics of power electronic devices.
2.	Construct the design and control of rectifiers, inverters.
3.	Discover of power electronic converters in power control applications.
4.	Compare characteristics of SCR, BJT, MOSFET and IGBT.
5.	Demonstrate communication methods.
6.	Experiment the design of AC voltage controller and Cyclo Converter.
7.	Construct the Chopper circuits.

Signature of HOD

Signature of faculty

Date:





Department of Electrical & Electronics Engineering

GUIDELINES TO STUDY THE COURSE / SUBJECT

Academic Year: 2018-2019Semester: IName of the Program:B.TechYear:III/ISection:BCourse/Subject:Power ElectronicCourse Code:GR15A3018Name of the Faculty:D KarunakumarDesignation:ASST.PROFESSOR.

Guidelines to study the Course/ Subject: Power Electronic

CourseDesignandDeliverySystem(CDD):

- The Course syllabus is written into number of learning objectives and outcomes.
- These learning objectives and outcomes will be achieved through lectures, assessments, assignments, experiments in the laboratory, projects, seminars, presentations, etc.
- Every student will be given an assessment plan, criteria for assessment, scheme of evaluation and grading method.
- The Learning Process will be carried out through assessments of Knowledge, Skills and Attitude by various methods and the students will be given guidance to refer to the text books, reference books, journals, etc.

The faculty be able to –

Understand the principles of Learning

Understand the psychology of students

Develop instructional objectives for a given topic



Department of Electrical & Electronics Engineering

Prepare course, unit and lesson plans

Understand different methods of teaching and learning

Use appropriate teaching and learning aids

Plan and deliver lectures effectively Provide feedback to students using various methods of Assessments and tools of Evaluation

Act as a guide, adviser, counselor, facilitator, and motivator and not just as a teacher alone

Signature of HOD faculty

Signature of

Date:

Date:



Department of Electrical & Electronics Engineering

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		COURSE	SCHED	ULE	
Academic Year		: 2018-2019			
Semester		: I			
Name of the	Program:	EEE	B.Tech	III/I	Section: B
Course/Subject:	Power Elect	ronic	Code	e: GR15A3018	3
Name of the Facul	lty: D.Karun	akumar		Dept:	EEE

Designation: Assistant professor The Schedule for the whole Course / Subject is:

Exp. No.	Description	Duration(Dat e)	Total No. of Periods
1.	Introduction to Power Semiconductor Devices	02-07-2018	2
2.	Thyristors, BJT, MOSFET and their characteristics	03-07-2018	2
3.	Basic theory of operation of Thyristors, Static V-I characteristics	04-07-2018	2
4.	Dynamic Characteristics, Thyristor Protection, Snubber circuit details	09-07-2018	2
5.	Turn-On & Off Methods, Two Transistor Analogy	10-07-2018	2
6.	Firing Circuit Model & UJT Triggering Circuit	11-07-2018	2
7	Series & Parallel operation ,Static Equalizing circuit	16-07-2018	2
8.	Dynamic Equalizing, Specifications and Ratings of SCR's	17-07-2018	2
9.	Line and Forced commutation circuit.	18-07-2018	2
10	Phase control technique, Single phase linecommutated converters	23-07-2018	2
11.	Half controlled converter with R-load, RL, RLE load	24-07-2018	2
12.	Half controlled converter with RL and Free wheeling Diode	25-07-2018	2
13.	Numerical problems & Performance parameters	30-07-2018	2



14.	Department of Electrical & Electronics Eng Fully controlled converter with R-load midpoint type,	31-07-2018	2
	Bridge type	51 57 2010	
15	Fully controlled converter with RL-load midpoint type,	01-08-2018	2
	Bridge type		
16	Fully controlled converter with RL-load midpoint type,Mid Point type	02-08-2018	2
17	Full controlled converters with RLE load and free wheeling	07-08-2018	2
17	diode	07-08-2018	
18	Active and Reactive power input, effect of source	08-08-2018	2
	inductance		
19	Introduction to dual converter	13-08-2018	2
20	Three phase bridge type converter with R-Load, RL-Load	14-08-2018	2
21	Three phase bridge type converter with RLE-Load, Bridge	20-08-2018	2
	point		
22	Three phase bridge type converter with RLE-Load Mid point	21-08-2018	2
23	Semi converter Effect of Source inductance Waveforms	27-08-2018	2
24	Inverters Single phase inverter Basic series inverter,	28-08-2018	2
25	Parallel Capacitor inverter, bridge inverter Waveforms,	29-08-2018	2
26	Voltage control techniques for inverters	10-09-2018	2
27	Pulse width modulation techniques Numerical problems.	11-09-2018	2
28	Basics of Resonant Inverters.	12-09-2018	2
29	AC voltage controllers Single phase two SCR's in	17-09-2018	2
	antiparallel with R		
30	AC voltage controllers 1-phase two SCR's in antiparallel with RL loads	18-09-2018	2
31	AC voltage controllers 1-phase two SCR's in antiparallel with RL loads	19-09-2018	2



Department of Electrical & Electronics Engineering

32	Triac with R and RL loads Derivation of RMS load voltage, current	24-09-2018	2
33	Triac with R and RL loads Derivation of RMS power factor- waveforms	25-09-2018	2
34	Cyclo converters Single phase mid point cyclo converters with R load	26-09-2018	2
35	Cyclo converters Single phase mid point cyclo converters with R& Load	01-10-2018	2
36	Choppers, Time ratio control and Current limit control strategies	03-10-2018	2
37	Step down choppers-Derivation of load voltage and currents with R Load	08-10-2018	2
38	Step down choppers-Derivation of load voltage and currents with R L Load	09-10-2018	2
39	Step down choppers-Derivation of load voltage and currents with RLE Load	10-10-2018	2
40	Morgan's chopper Jones chopper Oscillation choppers	15-10-2018	2
41	Waveforms AC Chopper Problems.	16-10-2018	2
42	Pulse Width Modulation Techniques	22-10-2018	2
43	Numerical problems	23-10-2018	2
44	Revision 5th Unit	24-10-2018	2
-			



Academic Year		TRUCTIONSCOURS	EPLAN
Semester	: I		
Name of the	Program: EEE	B.TechII/II	Section: B
Course/Subject:	Power Electronic	Code:GR15A3018	
Name of the Faculty: D.KarunakumarDept:EEEEEE.Designation: Assistant professor			

Exp. No	Topics	Objectiv es & Outcome s	References(TextBook,Journal)
1.	Introduction to Power Semiconductor Devices	1,2,3 & 1,-	. P.S.Bhimbra
2.	Thyristors, BJT, MOSFET and their characteristics	1,2,3 & 1,2	. P.S.Bhimbra
3.	Basic theory of operation of Thyristors, Static V-I characteristics	1,2,3& 1,2	. P.S.Bhimbra
4.	Dynamic Characteristics, Thyristor Protection, Snubber circuit details	1,2,3,6& 1,2	. P.S.Bhimbra
5.	Turn-On & Off Methods, Two Transistor Analogy	1,2,3& 1,2	. P.S.Bhimbra
6.	Firing Circuit Model & UJT Triggering Circuit	1,2,3 & 1,2	. P.S.Bhimbra
7	Series & Parallel operation ,Static Equalizing circuit	1,2,3,4& 1,2	. P.S.Bhimbra



	Department of Electrical & Ele	ectronics I	Engineering
8.	Dynamic Equalizing, Specifications and Ratings of SCR's	1,2,3 & 2	. P.S.Bhimbra
9.	Line and Forced commutation circuit.	1,2,3 & 2	. P.S.Bhimbra
10	Phase control technique, Single phase linecommutated converters	1,2,3& 2	. P.S.Bhimbra
11.	Half controlled converter with R-load,RL ,RLE load	1,2,3,& 2	. P.S.Bhimbra
12.	Half controlled converter with RL and Free wheeling Diode	1,2,3,4 ,5,6 & 2	. P.S.Bhimbra
13.	Numerical problems & Performance parameters	1,2,3 & 1,2	. P.S.Bhimbra
14.	Fully controlled converter with R-load midpoint type, Bridge type	1,2,3 & 1,2	. P.S.Bhimbra
15	Fully controlled converter with RL-load midpoint type, Bridge type	1,2,3& 1,2	. P.S.Bhimbra
16	Fully controlled converter with RL-load midpoint type, Mid Point type	1,2,3,6& 1,2	. P.S.Bhimbra
17	Full controlled converters with RLE load and free wheeling diode		. P.S.Bhimbra
18	Active and Reactive power input, effect of source inductance	1,2,3 & 1,2	. P.S.Bhimbra
19	Introduction to dual converter	1,2,3,4& 1,2	. P.S.Bhimbra
20	Three phase bridge type converter with R- Load, RL-Load	1,2,3 & 2	. P.S.Bhimbra
21	Three phase bridge type converter with RLE-Load, Bridge point	1,2,3 & 2	. P.S.Bhimbra
22	Three phase bridge type converter with RLE-Load Mid point	1,2,3& 2	. P.S.Bhimbra
	-		



Department of Electrical & Electronics Engineering				
23	Semi converter Effect of Source inductance Waveforms	1,2,3,& 2	. P.S.Bhimbra	
24	Inverters Single phase inverter Basic series inverter,	1,2,3,4 ,5,6 & 2	. P.S.Bhimbra	
25	Parallel Capacitor inverter, bridge inverter Waveforms,	1,2,3 & 1,2	. P.S.Bhimbra	
26	Voltage control techniques for inverters	1,2,3 & 1,2	. P.S.Bhimbra	
27	Pulse width modulation techniques Numerical problems.	1,2,3& 1,2	. P.S.Bhimbra	
28	Basics of Resonant Inverters.	1,2,3,6& 1,2	. P.S.Bhimbra	
29	AC voltage controllers Single phase two SCR's in antiparallel with R	1,2,3& 1,2	. P.S.Bhimbra	
30	AC voltage controllers 1-phase two SCR's in antiparallel with RL loads	1,2,3 & 1,2	. P.S.Bhimbra	
31	AC voltage controllers 1-phase two SCR's in antiparallel with RL loads	1,2,3,4& 1,2	. P.S.Bhimbra	
32	Triac with R and RL loads Derivation of RMS load voltage, current	1,2,3 & 2	. P.S.Bhimbra	
33	Triac with R and RL loads Derivation of RMS power factor- waveforms	1,2,3 & 2	. P.S.Bhimbra	
34	Cyclo converters Single phase mid point cyclo converters with R load	1,2,3& 2	. P.S.Bhimbra	
35	Cyclo converters Single phase mid point cyclo converters with R& Load	1,2,3,& 2	. P.S.Bhimbra	
36	Choppers, Time ratio control and Current limit control strategies	1,2,3,4 ,5,6 & 2	. P.S.Bhimbra	



Department of Electrical & Electronics Engineering

	Department of Electrical & Elec	ectronics I	Lingineering
27	Step down choppers-Derivation of load		. P.S.Bhimbra
37	voltage and currents with R Load	1,2,3 &	
		1,2	
20	Step down choppers-Derivation of load		. P.S.Bhimbra
38	voltage and currents with R L Load	1,2,3 &	
		1,2	
20	Step down choppers-Derivation of load		. P.S.Bhimbra
39	voltage and currents with RLE Load	1,2,3& 1,2	
40	Morgan's chopper Jones chopper Oscillation		. P.S.Bhimbra
40	choppers	1,2,3,6&	
	11	1,2	
41	Wayafarma AC Channar Brahlama	1,2,3& 1,2	. P.S.Bhimbra
41	Waveforms AC Chopper Problems.		
42			. P.S.Bhimbra
72	Pulse Width Modulation Techniques	1,2,3 & 1,2	
			. P.S.Bhimbra
43		1 2 2 4 0	
	Numerical problems	1,2,3,4&	
		1,2	
44	Revision 5th Unit	1 2 2 2 2	. P.S.Bhimbra
		1,2,3 & 2	

Signature of HOD

Signature of faculty

Date:

Date:





Department of Electrical & Electronics Engineering

COURSE OUTCOME AND PROGRAM OUTCOME MAPPING

PO's	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO's												
CO1	Н	Н	Н	Μ		Н		Μ	Н	Н	Н	Н
CO2		Н	Н	Μ		Н			Μ	Η	Η	Η
CO3	Н	Μ		Н		Μ	Н		Μ			Μ
CO4	Н		Н	Μ		Μ	Н	Μ	Μ		Н	Μ
CO5	Н	Н	Μ	Μ		Н	Н	Н			Н	Μ
CO6		Н	Н	Μ		Н	Н	Μ	Н	Μ	Н	Н
CO7	Н	Н	Н	Μ		Н		Μ	Н		Η	Η



Department of Electrical & Electronics Engineering

Assessment methods:

- 1. Operation skill and familiarization of software.
- 2. Experimental procedure, simulation results, internal observation, labrecord.
- 3. Internal examinations.
- 4. External examinations.
- 5. Viva-voce.

1. Course Objectives-Program Outcomes (POs) Relationship Matrix (Indicate the relationships by mark "X")

(indicate the re			-)	11 11	/							
P-Outcomes	А	В	c	d	e	F	g	h	i	j	k	1
C-Objectives												
1	Х	Х	Х	Х	Х				Х	Х	Х	Х
2	Х				Х		Х	Х		Х	Х	
3	Х	Х	Х			Х	Х	Х	Х		Х	Х
4				Х	Х	Х		Х	Х	Х	Х	
5		Х	Х	Х					Х	Х		
6				Х	Х	Х		Х		Х	Х	
7	Х	Х	Х	Х	Х	Х	Х		Х	Х	Х	

2. Course Outcomes-Program Outcomes (POs) Relationship Matrix (Indicate the relationships by mark"X")

anonompo og m		<u> </u>	1	1	1	1	1	1	1	1	1	1
P-Outcomes	а	b	c	d	e	f	g	h	i	J	Κ	1
C-Outcomes												
1	Х	Х	Х	Х	Х			Х	Х	Х	Х	Х
2	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
3	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
4	Х	Х	Х							Х	Х	Х
5	Х	Х	Х							Х	Х	Х
6	Х	Х	Х							Х	Х	Х
7	Х	Х	Х							Х	Х	Х

3. Courses (with title & code)-Program Outcomes (POs) Relationship Matrix

(Indicate the relationships by mark "X"



Department of Electrical & Electronics Engineering

P-Outcomes Courses	a	b	c	d	e	f	g	h	i	j	K	1
Electrical Networks Lab	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х

4. Program Educational Objectives (PEOs) –**Vision/Mission Matrix** (Indicate therelationships by mark "X")

		Mission of de	partment	
PEOs	Higher Learning	Contemporary Education	Technical knowledge	Research
Graduates will have a successful technical or professional careers, including supportive and leadership roles on multidisciplinary teams	Х	Х	Х	x
Graduates will be able to acquire, use and develop skills as required for effective professional practices		Х	Х	
Graduates will be able to attain holistic education that is an essential prerequisite for being a responsible member of society	Х		Х	
Graduates will be engaged in life- long learning, to remain abreast in their profession and be leaders in our technologically vibrant society.	Х		Х	X

5. Program Educational Objectives(PEOs)-Program Outcomes(POs) Relationship Matrix (Indicate the relationships by m

P- Outcome s PEOs	a	b	с	d	e	f
1	Х	Х	Х	Х	Х	





Department of Electrical & Electronics Engineering

2	Х	Χ	Х	Х	Х	
3		Х	Х	Х		Х
4				Х		

6.Course Objectives-Course Outcomes Relationship Matrix (Indicate the relationships by mark "X")

Course-Outcomes	1	2	3	4	5	6	7
Course-Objectives							
1	Х	X	X	Х	X	Х	Х
2	Х	X	X	Х	X	X	Х
3	X	Х					
4				X	X		
5			Х	Х	Х	X	Х
6			Х	Х	Х	Х	Х
7	Х		Х	Х	Х	X	

Program Educational Objectives (PEOs)-Course Outcomes Relationship Matrix (Indicate the relationships by mark

P-Objectives(PEO)	1	2	3	4
Course-Outcomes				
1	Х	Х		Х
2	Х	Х		Х
3	Х	Х		Х
4	Х	Х		Х
5	Х	Х		Х
6	Х	Х		Х
7	Х	Х		Х

8. Assignments & Assessments-Program Outcomes (POs) Relationship Matrix (Indicate the relationships by mark "X"

P-Outcomes	А	b	c	d	e	f
Assessments						
1	Х	х		Х		x
2	Х	x	x			x



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3	Х	х	x	Х
4	Х	х	х	х

9. Assignments & Assessments-Program Educational Objectives (PEOs) Relationship Matrix (Indicate the relationships by

P-Objectives (PEOs) Assessments	1	2	3	4
1	Х	Х		
2		Х		
3		Х	Х	Х
4		Х		
5		Х		

Assessment process and Relevant Surveys conducted:

1. Constituencies -Program Outcomes (POs) Relationship Matrix (Indicate the relationships by mark "X"). Constituencies

- 1. Alumni
- 2. Governmentemployers
- 3. Students

P-Outcomes	а	b	c	d	e	f	G	h	i	j	k	1
Constituencies												
1	Х	Х	Х	Х	Х	Х	Х		Х	Х		Х
2	Х	Х	Х	Х	Х	Х	Х		Х			Х
3	Х	Х			Х	Х	Х	Х		Х	Х	Х

9 CO-Cognitive Level Mapping

Subject : Power Electronic

СО	Cognitive Lo					
	1	2	3	4	5	6
1		Х				
2			Х			
3						Х
4				Х		



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5	_	Х			
6			Х		
7		Х			

Cognitive Learning Levels:

CLL1: Remembering

CLL2: Understanding

CLL3: Applying

CLL4: Analyzing

CLL5: Evaluating

CLL6: Creating



Department of Electrical & Electronics Engineering

Academic Year	EVALUATION STRAT : 2018-2019	ſEGY
Semester	: I	
Name of the Program:	EEE B.Tech	III/I Section: B
Course/Subject: Power El	ectronic Co	de: GR15A3018
Name of the Faculty: D.Ka	runakumar	Dept:EEE
Designation: Assistant pr	ofessor	
1. TARGET:		
A) Percentage for pass:	100%	
2. COURSE PLAN & CO	ONTENT DELIVERY	
• PPT presentation	of the Lectures	
• Solving exercise r	problems	
• Model questions		
3. METHOD OF EVALU	JATION	
3.1 Daily Attendan	ce	
$3.2 \square$ Lab records an	d observation	
3.3 Mini Projects		
3.4 🗆 Viva Voce		
3.5 Internal Exami	nation	
3.6 Semester/End	Examination	

4. List out any new topic(s) or any innovation you would like to introduce in teaching the subjects in this Semester.

Signature of HOD	Signature of faculty
Date:	Date:



Department of Electrical & Electronics Engineering

RUBRIC

OBJECTIVE: Work effectively with others

STUDENT OUTCOME: Ability to function in a multi-disciplinary team

S.No.	Student Name	Performance Criteria	Unsatisfactory	Developing	Satisfactor Y	Exemplar y	Scor e
			1	2	3	4	
1.	INDURI PAVANI (17241A0274)	Research & Gather Information	Does not collect any information that relates to	Collects very little information some relates	Collects some basic Informatio n most	Collects a great deal of Informati on all	
			the topic.	to the topic	relates to the topic.	relates to the topic.	
		Fulfill team role's	Does not perform any duties of assigned team role.	Performs very little duties.	Performs nearly all duties.	Performs all duties ofassigne d team role.	
		Share Equally	Always relies on others to do the work.	Rarely does the assigned work often needs reminding.	Usually does the assigned work rarely needs reminding.	Always does the assigned work without having to be reminded	



				5	
	Listen to other team mates	Is always talkingnever allows anyone else to speak.	Usually doing most of the talking rarely allows others to	Listens, but sometimes talks too much.	Listens and speaks a fair amount.
			speak.		
					Average score
PUDOTA ADITYA CECIL RAJ 2. (16241A02A0)	Research & Gather Information	Does not collect any information that relates to the topic.	Collects very little information some relates to the topic	Collects some basic informatio nmost relates to the topic.	Collects a great deal of informati onall relates to the topic.
	Fulfill team role's	Does not perform any duties of assigned team role.	Performs very little duties.	Performs nearly all duties.	Performs all duties of assigned team role.
	Share Equally	Always relies on others to do	Rarely does the assigned	Usually does the assigned	Always does the assigned



		the work.	work often needs reminding.	work rarely needs reminding.	work without having to be reminded	
	Listen to other team mates	Is always talkingnever allows anyone else to speak.	Usually doing most of the talking rarely allows others to	Listens, but sometimes talks too much.	Listens and speaks a fair amount.	
K VAISHNAVI			speak.		Average score	
3 (17245A0214)	Research & Gather Information	Does not collect any information that relates to the topic.	Collects very little information some relates to the topic	Collects some basic informatio nmost relates to the topic.	Collects a great deal of informati onall relates to the topic.	
	Fulfill team role's	Does not perform any duties of assigned team role.	Performs very little duties.	Performs nearly all duties.	Performs all duties of assigned team role.	



			Ŭ		
Share Equally	Always relies on others to do the work.	Rarely does the assigned work often needs reminding.	Usually does the assigned work rarely needs reminding.	Always does the assigned work without having to be reminded	
Listen to other team mates	Is always talkingnever allows anyone else to speak.	Usually doing most of the talking rarely allows others to speak.	Listens, but sometimes talks too much.	Listens and speaks a fair amount.	
				Average score	



Department of Electrical & Electronics Engineering

COURSE COMPLETION STATUS

Academic Year	: 2018-2019		
Semester	: I		
Name of the Program:	EEE B.Tech	III/I	Section: B
Course/Subject: Power Elec	ctronic Co	ode: GR15A30	18
Name of the Faculty: D.Karu	unakumar D	Dept:	EEE

Designation: Assistant professor

Progra m	Remarks	No. of Objectives Achieved	No. of Outcomes Achieved
1	1 st unit completed by 18/07/18	1,3	1,4
2	2^{nd} unit completed by $13/08/18$	2,3	3,4
3	3 rd unit completed by 12/09/18	4,3	2,3
4	4 th unit completed by 08/10/18	5,3	4,5
5	5 th unit completed by 23/10/19	1,3	2,4

Signature of HOD

Date:

Signature of faculty

Date:

Note: After the completion of each unit mention the number of Objectives & Outcomes Achieved.



Department of Electrical & Electronics Engineering

GUIDELINES TO STUDY THE COURSE/SUBJECT

Academic Year	: 2018-2019		
Semester	: I		
Name of the Program:	EEE B.Tech	III/I	Section: B
Course/Subject: Power E	lectronic	Code: GR15A3	018
Name of the Faculty: D.Ka	arunakumar	Dept:	EEE
Designation: Assistant pr	ofessor		

Course Design and Delivery System (CDD):

- □ The Course syllabus is written into number of learning objectives and outcomes.
- □ These learning objectives and outcomes will be achieved through lectures, assessments, assignments, experiments in the laboratory, projects, seminars, presentations, etc.
- □ Every student will be given an assessment plan, criteria for assessment, scheme of evaluation and grading method.
- □ The Learning Process will be carried out through assessments of Knowledge, Skills and Attitude by various methods and the students will be given guidance to refer to the text books, reference books, journals, etc.

The faculty be able to –

- □ Understand the principles of Learning
- □ Understand the psychology of students
- □ Develop instructional objectives for a given topic
- □ Prepare course, unit and lesson plans
- □ Understand different methods of teaching and learning
- □ Use appropriate teaching and learning aids
- □ Plan and deliver lectures effectively
- □ Provide feedback to students using various methods of Assessments and tools of Evaluation
- □ Act as a guide, advisor, counselor, facilitator, motivator and not just as a teacher alone

Signature of HOD Date:

Signature of faculty Date:



Department of Electrical & Electronics Engineering

Result Analysis

B.Tech EEE III YEAR I SEM RESULT ANALYSIS OF 2016-2020 BATCH

ACADEMIC YEAR 2018-2019

TOTAL. NO. OF STUDENTS REGISTERED = 142

	Total No. of	No. of student	No. of student			Grad	le Poi	ints			
Subject	students appeare d	s passed	s failed	< 5	5	6	7	8	9	10	Pass percent age
MC	142	116	26	07	13	15	20	32	27	02	81.69%
MC Lab	142	141	01	00	01	00	00	09	26	105	99.29%
PTS	142	128	14	01	12	12	14	30	34	25	90.14%
EMI	142	128	14	08	11	08	12	32	31	26	90.14%
PE	142	135	07	03	08	11	08	27	37	41	95.07%
SMI Lab	142	140	02	06	10	02	04	12	17	89	98.59%
PE Lab	142	140	02	00	01	02	07	27	31	72	98.59%
SWE	142	125	17	06	11	16	09	44	29	10	88.02%

Overall pass (passed in all subjects) = 107/142 (75.35%)

Power Transmission System	V Vijaya Rama Raju, M Prashanth
Microcontrollers	P Prashanth Kumar
Electrical Measurements& Instrumentation	U Vijaya Lakshmi
Power Electronics	Dr T Suresh Kumar,D Karuna Kumar



Department of Electrical & Electronics Engineering

Solar and Wind Energy	P Sri Vidya Devi /Dr J Praveen
Systems	
Sensors/Measurements& Instrumentation Lab	P Srividya Devi/U Vijaya Lakshmi/P Sirisha
Power Electronics Lab	Dr T Suresh Kumar/Syed Sarfaraz Nawaz/M Rekha
Microcontrollers Lab	R Anil Kumar/MN Sandhya Rani

ARREARS POSITION – CURRENT YEAR

Descri	All	One	Two	Three	More than	% of
ption	pass	Arrear	Arrears	Arrears	Three Arrears	pass
142	107	10	16	03	06	75.35%

Performance overall Class Three Toppers

16241A0259		
	VIPPARTHI SOWMYA	10
16241A0274		
16241A0290		
17245A0205		
17245A0214	INDURI PAVANI MANGANAPALLY ROOPA	9.84
17245A0221	CHILUKA PRANAVI	
	K VAISHNAVI	
	P SWATHI	
16241A0257		
	UNDETY MOUNIKA	9.72

HOD,EEE

S.NO	and the second se	FACULTY ID FACULTY NAME	SUBJECT NAME	DEPT	NO. OF SECTIONS	FEEDBACK 1 (4 POINTS) (AVG OF ALL SECTIONS)
-	361	V.Vijaya Rama Raju	Power Transmission System	EEE	6	UE E
N	1279	M Prashanth	Power Transmission System	EEE	C	00° C
0	1055	P Prashanth Kumar	Microcontrollets	REE	6	3.37
4	1494	Dr T Suresh Kumar	Power Electronics	EEE	-	3.31
un	760	D Karuna Kumar	Power Electronics	BEE	1	3.20
9	692	U Vijaya Lakshmi	Electrical Measurements and Instrumentation	EEE	2	3.24
-	931	P Sri Vidya Devi	Solar & Wind Energy Systems	EEE	2	3.12
0	931	P Sri Vidya Devi	Sensors/Measurements and Instrumentation Lab	EEE	1	3.39
10	692	U Vijaya Lakshmi	Sensors/Measurements and Instrumentation Lab	EEE	1	3.53
11	934	P Sirisha	Sensors/Measurements and Instrumentation Lab	BBB	2	3.41
12	695	Syed Sarfaraz Nawaz	Power Electronics Lab	EEE	1	3,11
13	933	M Rekha	Power Electronics Lab	EEE	2	3,19
14	609	P Praveen Kumar	Power Electronics Lab	EEE	1	3.55
15	657	R. Anil Kumar	Microcontrollers Lab	EEE	1	3.31
16	760	D Karuna Kumar	Microcontrollers Lab	REE	2	3.31
12	1055	P Prashanth Kumar	Microcontrollers Lab	EEE	1	3.20



	CO Attainment for	· All Mid	s.				
	Gokaraju Rangaraju Institute of Engineering & Technology						
D	Dept: EEE III year MID-I Academic Year:2018-19 I Sem						
	Subject Name: Power Electronics Date: 04.09.2018						
Course Attainment Analysis							
Roll Numbers	Name	Q1 [5M] CO4	Q2 [5M] CO1	Q3 [5M] CO5	Q4 [5M] CO2		
16241A0261	A PRASHANTH	5	5	4			
16241A0262	ADEPU SOWMYA	5	5		5		
16241A0263	AMGOTH RISHITHA PAMAAR	5	5		5		
16241A0264	ARVIND NAIDU	4	2				
16241A0265	BOLISHETTI SAIJEEVAN	5					
16241A0266	BOLLUR YASHWANT	5		2	3		
16241A0267	BOMRASPET PHANIDER	5	5		5		
16241A0268	CHALLAGUNDLA SOWMYA	5	5		2		
16241A0269	CHINTAPOOLA SWATHI	5	5	5	5		
16241A0270	DESHPANDE PRAVALIKA	AB	AB	AB	AB		
16241A0271	GONE SOWMYA	5		4	4		
16241A0272	GOPIDI VENKAT REDDY	5	5	4	5		
16241A0273	GORENKALA MEGHA SAIKRISHNA	2	2		3		
16241A0274	INDURI PAVANI	5	5	5	5		
16241A0275	JALAMANCHILI RAMA SURYAM	5	5	5			
16241A0276	JONNAVALASA DEVI PRASAD	5	5		4		
16241A0277	K V S SANDEEP	3			1		
16241A0278	KALYANAPU VENUGOPAL	5	4		5		
16241A0279	KANNE SACHIN	2		3			
16241A0280	KARAM SANDHYARANI	5	5	5	4		
16241A0281	KATTA MOUNIKA	5	5		4		
16241A0282	KIDAMBI SREE GOVIND	5	5		5		
16241A0283	KOLLIPARA CHAITANYA SAI	5	5		1		
16241A0284	KONDA ANIL KUMAR	5		2	5		



	Department of Electrical & Ele	ctronics	Enginee	ering	
16241A0285	KUNCHALA MOHANBABU	5		5	5
16241A0286	LANKA ROHITHA SRI	5	1	4	5
16241A0287	MADAPATHI SACHIN	5	2		
16241A0288	MALAKA UDAYASAGAR	4		1	
16241A0289	MALAVATH JAIPAL	4	4		5
16241A0290	MANGANAPALLY ROOPA	5	5		5
16241A0291	MOHAMMED KHALEEL	5	5		5
16241A0292	MUKKAMULA RAMYA SREE	5		4	4
16241A0293	MUNDRA SUBHASHINI	5			5
16241A0294	MYSA VINOD KUMAR	5			
16241A0295	NAGARAM VAMSHI	4		2	2
16241A0296	NAGARAPU PRADEEP		1		2
16241A0297	PATHAPATI DIVYA	5	2	2	4
16241A0298	POTTA SURYATEJA	3			4
16241A0299	PRODDUTUR MOHAN SAI	4			5
16241A02A0	PUDOTA ADITYA CECIL RAJ	2			5
16241A02A2	SADANAVENA RAHUL		4	4	5
16241A02A3	SAI TEJASWI NOOKA	5	5	3	
16241A02A4	SAKETH M	5	5		5
16241A02A5	SANGEM SOUJANYA	5	5	5	
16241A02A6	SANGISETTY RAKESH SAGAR		3	1	2
16241A02A7	SHASTRALA SRAVYA	5	5		5
16241A02A8	SURAM SHIRISHA	5	5		5
16241A02A9	SURYA SANJAY BANDARI	5	5		
16241A02B0	T LAKSHMI ASRITH	3	1		4
16241A02B1	TERATPALLY YESHWANTH	5	5		5
16241A02B2	THELLA SAI KRISHNA	5	2	3	
16241A02B3	THOTAKURI VISHAL	5	2		
16241A02B4	TUMMALACHARLA PRAVEEN	5		4	5
16241A02B5	VANGA RITHVIKA	5	5		
16241A02B6	VIDYA KANURI	5	5		4
	VINEESHA SRAVYA LAKSHMI .	_	_		
16241A02B7	B	5	5		5
16241A02B8	VUJJINI HARSHITHA	5		4	5
16241A02B9	BHANU KAUSTUBA WALTATI	3		2	
17245A0213	K RAGHAVENDER	5		5	5



Department of Electrical & Ele	cuomes.	Enginee	iiiig	
K VAISHNAVI	5		5	5
MANNELI KRANTHI KUMAR	5		3	5
MARTHA REVAN KUMAR	4			5
MASANNAGARI RAKESH REDDY	4		2	4
NARSING SHRAVANI	5	4	5	5
PONNAM ADITHYA	5		5	4
POOSALA NAVYARANI	5		5	5
P SWATHI	5		5	5
SABAVATH PARAMESH	5		5	5
SHAIK ASIF AHMED	5		4	5
SHAIK SOHEL	5		5	5
Grand Total	306	164	132	235
NSA	66.0	40.0	35.0	54.0
Attempt %=(NSA/Total no of students)*100	94.3	57.1	50.0	77.1
Average (attainment)= Total/NSA	4.6	4.1	3.8	4.4
Attainment%= (Avg/max. Marks for question)*100	92.73	82.00	75.43	87.04
	CO4	CO1	CO5	CO2
	CO1	81.5		
	CO2	86.6		
	CO4	92.73		
	K VAISHNAVI MANNELI KRANTHI KUMAR MARTHA REVAN KUMAR MASANNAGARI RAKESH REDDY NARSING SHRAVANI PONNAM ADITHYA POOSALA NAVYARANI P SWATHI SABAVATH PARAMESH SHAIK ASIF AHMED SHAIK SOHEL Grand Total NSA Attempt %=(NSA/Total no of students)*100 Average (attainment)= Total/NSA Attainment%= (Avg/max. Marks)	K VAISHNAVI5MANNELI KRANTHI KUMAR5MARTHA REVAN KUMAR4MASANNAGARI RAKESH REDDY4NARSING SHRAVANI5PONNAM ADITHYA5POOSALA NAVYARANI5P SWATHI5SABAVATH PARAMESH5SHAIK ASIF AHMED5SHAIK SOHEL5Grand Total306Attempt %=(NSA/Total no of students)*10094.3Average (attainment)= Total/NSA4.6Attainment%= (Avg/max. Marks for question)*10092.73CO4CO1CO2CO2	K VAISHNAVI5MANNELI KRANTHI KUMAR5MARTHA REVAN KUMAR4MASANNAGARI RAKESH REDDY4NARSING SHRAVANI5PONNAM ADITHYA5POOSALA NAVYARANI5P SWATHI5SABAVATH PARAMESH5SHAIK ASIF AHMED5SHAIK SOHEL5Grand Total306Attempt %=(NSA/Total no of students)*10094.3Average (attainment)= Total/NSA4.64.1Attainment%= (Avg/max. Marks for question)*10092.73CO181.5CO286.6	MANNELI KRANTHI KUMAR53MARTHA REVAN KUMAR41MASANNAGARI RAKESH REDDY42NARSING SHRAVANI54555PONNAM ADITHYA55POOSALA NAVYARANI55P SWATHI55SABAVATH PARAMESH55SHAIK ASIF AHMED54SHAIK SOHEL55Grand Total306164NSA66.040.0Attempt %=(NSA/Total no of students)*10094.357.1Attainment%= (Avg/max. Marks for question)*10092.7382.00CO181.5CO286.6



Gokaraju Rangaraju Institute of Engineering & Technology								
De	ept: EEE III year MID-II Aca	demic Y	ear:2018	-19 I Se	em			
	Subject Name: Power Electronics							
	Date: 25.10.2018							
Course Attainment Analysis								
Roll Numbers	Name	Q1 [5M] CO2	Q2 [5M] CO6	Q3 [5M] CO6	Q4 [5M] CO7			
16241A0261	A PRASHANTH	5	4		4			
16241A0262	ADEPU SOWMYA	5	5	5				
16241A0263	AMGOTH RISHITHA PAMAAR	5	5	5				
16241A0264	ARVIND NAIDU	4	4		4			
16241A0265	BOLISHETTI SAIJEEVAN	4	3	4				
16241A0266	BOLLUR YASHWANT	4	4					
16241A0267	BOMRASPET PHANIDER	5	5	4				
16241A0268	CHALLAGUNDLA SOWMYA	5	5	2				
16241A0269	CHINTAPOOLA SWATHI	5	5	5	5			
16241A0270	DESHPANDE PRAVALIKA	4	5	5				
16241A0271	GONE SOWMYA	5	5	4				
16241A0272	GOPIDI VENKAT REDDY	5	5	5				
16241A0273	GORENKALA MEGHA SAIKRISHNA	3	3	4				
16241A0274	INDURI PAVANI	5	5	5	2			
16241A0275	JALAMANCHILI RAMA SURYAM	5	5	5				
16241A0276	JONNAVALASA DEVI PRASAD	5	5	5				
16241A0277	K V S SANDEEP		5					
16241A0278	KALYANAPU VENUGOPAL	5	5	5				
16241A0279	KANNE SACHIN	4	5	2				
16241A0280	KARAM SANDHYARANI	5	5	5				
16241A0281	KATTA MOUNIKA	5	5	5				
16241A0282	KIDAMBI SREE GOVIND	5	5	5				
16241A0283	KOLLIPARA CHAITANYA SAI		4	3				
16241A0284	KONDA ANIL KUMAR	5	5	5				



	Department of Electrical & Ele		Enginee	inig	1
16241A0285	KUNCHALA MOHANBABU	5	5	5	
16241A0286	LANKA ROHITHA SRI	4	5	4	
16241A0287	MADAPATHI SACHIN		5	5	
16241A0288	MALAKA UDAYASAGAR		5		
16241A0289	MALAVATH JAIPAL		5	5	5
16241A0290	MANGANAPALLY ROOPA		5	5	5
16241A0291	MOHAMMED KHALEEL	5	5	5	
16241A0292	MUKKAMULA RAMYA SREE	4	4	4	
16241A0293	MUNDRA SUBHASHINI	4	5	2	
16241A0294	MYSA VINOD KUMAR	4		4	
16241A0295	NAGARAM VAMSHI	3	3	4	
16241A0296	NAGARAPU PRADEEP	5	5	5	
16241A0297	PATHAPATI DIVYA	5	5	5	
16241A0298	POTTA SURYATEJA	3			
16241A0299	PRODDUTUR MOHAN SAI	5		5	5
16241A02A0	PUDOTA ADITYA CECIL RAJ		4		3
16241A02A2	SADANAVENA RAHUL	5	5		5
16241A02A3	SAI TEJASWI NOOKA	5	5		4
16241A02A4	SAKETH M	5	5	4	
16241A02A5	SANGEM SOUJANYA	5	5	5	
16241A02A6	SANGISETTY RAKESH SAGAR	4			
16241A02A7	SHASTRALA SRAVYA		5	5	5
16241A02A8	SURAM SHIRISHA	5	5		5
16241A02A9	SURYA SANJAY BANDARI		5	5	
16241A02B0	T LAKSHMI ASRITH	5	5	4	
16241A02B1	TERATPALLY YESHWANTH	5	5	5	
16241A02B2	THELLA SAI KRISHNA	5	5	5	
16241A02B3	THOTAKURI VISHAL	5		2	
16241A02B4	TUMMALACHARLA PRAVEEN	5	5	5	
16241A02B5	VANGA RITHVIKA	5	5	1	4
16241A02B6	VIDYA KANURI	5	5	3	
	VINEESHA SRAVYA LAKSHMI .				
16241A02B7	B	5	5	5	
16241A02B8	VUJJINI HARSHITHA		5	5	5
16241A02B9	BHANU KAUSTUBA WALTATI	4	3		
17245A0213	K RAGHAVENDER	5	5	5	



Department of Electrical & Electronics Engineering					
17245A0214	K VAISHNAVI	5	5	5	
17245A0215	MANNELI KRANTHI KUMAR	5	5	5	
17245A0216	MARTHA REVAN KUMAR	5	4	4	
17245A0217	MASANNAGARI RAKESH REDDY	4	4	5	
17245A0218	NARSING SHRAVANI	5	4	5	5
17245A0219	PONNAM ADITHYA	5	5		5
17245A0220	POOSALA NAVYARANI	5	5	5	
17245A0221	P SWATHI	5	5	5	
17245A0222	SABAVATH PARAMESH	5	5	5	
17245A0223	SHAIK ASIF AHMED	5	5	4	
17245A0224	SHAIK SOHEL	5	5	4	
18248A0201	K ALHILA	4	4	4	5
	Grand Total	282	308	252	71
	NSA	60.0	65.0	57.0	16.0
	Attempt %=(NSA/Total no of students)*100	84.5	91.5	80.3	22.5
	Average (attainment)= Total/NSA	4.7	4.7	4.4	4.4
	Attainment%= (Avg/max. Marks for question)*100	94.00	94.77	88.42	88.75
		CO2	94		
		CO6	91.60		
		CO7	88.75		

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